

LVT Logic Low-Voltage Technology

A 5-V Tolerant, 3.3-V Line of Products

Data Book

1998

Logic Products

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The SNZ4LVTH16500, SNS4LVTH16501, SNZ4LVTH16501, and SNZ4LVTH16835 are shown as product preview in this data book. The corresponding production data LVT data sheets for those devices are evaluable through the Ti home page at http://wwii.com/.

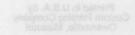
LVT Widebus"
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The SN74LVTH16500, SN54LVTH16501, SN74LVTH16501, and SN74LVTH16835 are shown as product preview in this data book. The corresponding production data LVT data sheets for these devices are available through the TI home page at http://www.ti.com/.

LVT Logic Low-Voltage Technology Data Book

A 5-V Tolerant, 3.3-V Line of Products

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INTRODUCTION

The 3.3-V LVT family uses the latest 0.8-μ BiCMOS process technology with performance specifications ideal for networking and telecommunication applications. In addition to popular octal and Widebus™ bus-interface devices, Texas Instruments (TI™) also offers the universal bus transceiver (UBT™) in this low-voltage family.

Performance characteristics of the LVT family are:

- Speed Provides high performance with maximum propagation delays of 3.5 ns for buffers.
- 3.3-V Operation With 5-V Tolerant I/Os Capability to interface with a mixed-voltage environment. The I/Os can handle up to 7 V, which allows them to act as 5-V to 3-V translators.
- High Drive/Low Power The LVT family provides up to 64 mA of drive, yet consumes less than 100 μA of standby power at 3.3-V V_{CC}.

Additional features include:

- Live Insertion LVT devices incorporate circuitry to protect the devices in live-insertion
 applications. The devices go into the high-impedance state during power up and power down
 [power-up 3-state (PU3S)].
- Bus Hold Bus hold prevents floating inputs by holding inputs at the last valid logic state. This eliminates the need for external pullup and pulldown resistors.
 - Damping-Resistor Option TI implements series-damping resistors on selected devices, which reduces overshoot and undershoot and helps match the line impedance to minimize ringing.
 - Packaging LVT devices are available in packaging options, such as small-outline integrated circuit (SOIC), shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), and thin very small-outline package (TVSOP) for octal and Widebus devices.

Some of the information in this data book is product preview. More information is available on these products, including availability dates, pricing, and final timing specifications. Please contact your local TI representative, authorized distributor, the TI technical support hotline at 972-644-5580, or visit the TI home page at http://www.ti.com.

TI also offers a complete line of low-voltage CMOS products, including Advanced Low-Voltage CMOS (ALVC), Low-Voltage CMOS (LVC), and Low-Voltage HCMOS (LV). For a complete listing of these and other TI logic solutions, please order the Logic Selection Guide (literature number SDYU001) by calling the literature response center at 1-800-477-8924.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

0	Immed	aanaaitanaa
Ci	Input	capacitance

The internal capacitance at an input of the device

Cio Input/output capacitance

Input-to-output internal capacitance; transcapacitance

Co Output capacitance

The internal capacitance at an output of the device

C_{pd} Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):

 $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

f_{max} Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that

should cause changes of output logic level in accordance with the specification

I_{CC} Supply current

The current into* the V_{CC} supply terminal of an integrated circuit

△I_{CC} Supply current change

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than

0 V or Vcc

ICEX Output high leakage current at a set of the output of the sum below test

The maximum leakage current into the collector of the pulldown output transistor when the output is high

and the output forcing condition $V_0 = 5.5 \text{ V}$

I_{I(hold)} Input hold current

Input current that holds the input at the previous state when the driving device goes to a

high-impedance state

I_{IH} High-level input current

The current into* an input when a high-level voltage is applied to that input

I_{IL} Low-level input current

The current into* an input when a low-level voltage is applied to that input

Input/output power-off leakage current

The maximum leakage current into/out of the input/output transistors when forcing the input/output to

4.5 V and $V_{CC} = 0 \text{ V}$

IOH High-level output current

The current into* an output with input conditions applied that, according to the product specification,

establishes a high level at the output

*Current out of a terminal is given as a negative value.



I_{OL} Low-level output current

The current into* an output with input conditions applied that, according to the product specification, establishes a low level at the output

I_{OZ} Off-state (high-impedance-state) output current (of a 3-state output)

In The current that flows through the output gates when the devcie is in the high-impedance state

I_{OZPU} The current that flows into or out of the output stage when the device is being powered up from the high-impedance state

I_{OZPD} The current that flows into or out of the output stage when the device is being powered down from the high-impedance state

ta Access time

The time interval between the application of a specified input pulse and the availability of valid signals at an output

t_c Clock cycle time

Clock cycle time is 1/fmax.

t_{dis} Disable time (of a 3-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ} . Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

t_{en} Enable time (of a 3-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low)

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{\text{OE}}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL} . Open-collector outputs change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

th Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

t_{pd} Propagation delay time

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{pLH})

t_{PHL} Propagation delay time, high-to-low level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

^{*}Current out of a terminal is given as a negative value.



tpHZ Disable time (of a 3-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

t_{PLH} Propagation delay time, low-to-high level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

t_{PLZ} Disable time (of a 3-state output) from low level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

t_{PZH} Enable time (of a 3-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

tpzL Enable time (of a 3-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

t_{sk(o)} Output skew

The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching output. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.

t_{su} Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

- NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.
 - 2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is to be expected.

t_w Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

∆t/∆v Input voltage transition rate

The input transition rise or fall rate corresponding to the change in signal amplitude with time

∆t/∆V_{CC} Power supply power-up rate

The power-up ramp rate corresponds to the transition rate of the supply voltage when the device is being powered up.

VIH High-level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.



V_{IL}

Low-level input voltage

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

VoH

High-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output

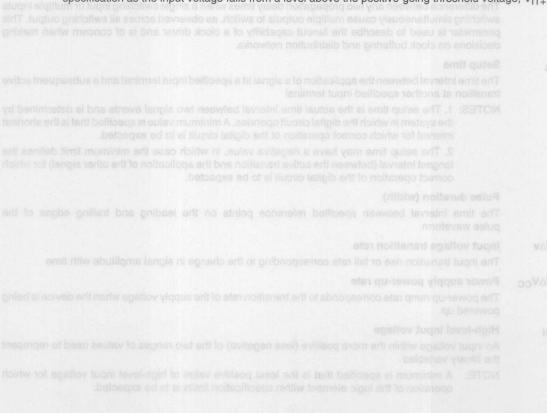
VoL

Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output

Positive-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{IT+}





VIT+

VIT-

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H = high level (steady state)

L = low level (steady state)

transition from low to high level

= transition from high to low level

= value/level or resulting value/level is routed to indicated destination

= value/level is re-entered

X = irrelevant (any input, including transitions)

Z = off (high-impedance) state of a 3-state output

a . . . h = the level of steady-state inputs A through H, respectively

Q₀ = level of Q before the indicated steady-state input conditions were established

= complement of Q₀ or level of Q̄ before the indicated steady-state input conditions were established

Q_n = level of Q before the most recent active transition indicated by ↓ or ↑

__ = one high-level pulse

= one low-level pulse

Toggle = each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid when the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with \uparrow and/or \downarrow , this means the output is valid when the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q₀, or \overline{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction of those shown have no effect at the output. (If the output is shown as a pulse, $\neg \neg \neg \neg \neg$, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)



EXPLANATION OF FUNCTION TABLES

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register.

FUNCTION TABLE

				INPUTS			level	rigiri	OF WG	mon	OUTI	PUTS	
OLEAD	MC	DE	OLOOK	SEI	RIAL	1	PARA	LLEL	at rigin	from	io diane	0-	0-
CLEAR	S1	SO	CLOCK	LEFT	RIGHT	Α	В	C	D	QA	QB	QC	QD
L	X	X	X	X	X	X	X	X	X	n di io	vallauk	V L	L
Н	X	X	L	X	X	X	X	X	X	QAO	Q _{B0}	QCO	Q _{D0}
Н	Н	Н	1	X	X	a	b	С	d	a	b	С	d
Н	L	Н	1	X	Н	Н	Н	Н	Н	Н	QAn	Q _{Bn}	QCn
Н	L	Н	1	X	L	L	L	L	L	L	Q _{An}	Q _{Bn}	QCn
Н	Н	L C	↑	Н	X	X	X	X	X	QBn	QCn	QDn	Н
Н	Н	ni gia	1	percolt	X	X	X	X	X	Q _{Bn}	QCn	QDn	L
Н	L	L	X	X	X	X	X	X	X	QAO	Q _{B0}	QCO	Q _{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low, regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that as long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Because on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs occurs while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, regardless of the serial input, the data entered at A is at output Q_A , data entered at B is at Q_B , and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B , the previous levels of Q_B and Q_C are now at Q_C and Q_D , respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A , the previous levels of Q_C and Q_D are now at Q_B and Q_C , respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

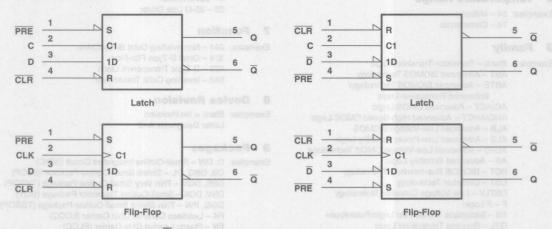
The function-table functional tests do not reflect all possible combinations or sequential modes.



It is TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \overline{Q} . An input that causes a Q output to go high or a \overline{Q} output to go low is called preset (PRE). An input that causes a \overline{Q} output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and \overline{CLR}) if they are active low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits \overline{D} and Ω

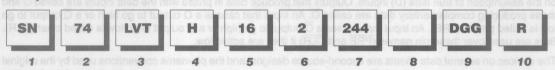
In some applications, it may be advantageous to redesignate the data input from D to \overline{D} or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and \overline{Q} exchange names, the preset and clear pins also exchange names. The polarity indicators (\searrow) on \overline{PRE} and \overline{CLR} remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or \overline{D}), Q, and \overline{Q} . Pin 5 (Q or \overline{Q}) is still in phase with the data input (D or \overline{D}); their active levels change together.



Example:



1 Standard Prefix

Example: SNJ - Conforms to MIL-PRF-38535 (QML)

2 Temperature Range

Examples: 54 - Military

74 - Commercial

3 Family

Examples: Blank - Transistor-Transistor Logic

ABT – Advanced BiCMOS Technology

ABTE – Advanced BiCMOS Technology/ Enhanced Transceiver Logic

AC/ACT – Advanced CMOS Logic

AHC/AHCT - Advanced High-Speed CMOS Logic

ALB – Advanced Low-Voltage BiCMOS ALS – Advanced Low-Power Schottky Logic

ALVC - Advanced Low-Voltage CMOS Technology

AS - Advanced Schottky Logic

BCT – BiCMOS Bus-Interface Technology

CBT - Crossbar Technology

CBTLV - Low-Voltage Crossbar Technology

F-F Logic

FB - Backplane Transceiver Logic/Futurebus+

GTL - Gunning Transceiver Logic

HC/HCT - High-Speed CMOS Logic

HSTL - High-Speed Transistor Logic

LS - Low-Power Schottky Logic

LV - Low-Voltage HCMOS Technology

LVC - Low-Voltage CMOS Technology

LVT - Low-Voltage BiCMOS Technology

S - Schottky Transistor-Transistor Logic

SSTL - Stub Series-Terminated Logic

4 Special Features

Examples: Blank = No Special Features

D - Level-Shifting Diode (CBTD)

H - Bus Hold (ALVCH)

R - Damping Resistor on Inputs/Outputs (LVCR)

S - Schottky Clamping Diode (CBTS)

5 Bit Width

Examples: Blank = Gates, MSI, and Octals

1G - Single Gate

8 - Octal IEEE 1149.1 (JTAG)

16 - Widebus™ (16, 18, and 20 bit)

18 - Widebus IEEE 1149.1 (JTAG)

32 - Widebus+™ (32 and 36 bit)

6 Options

Examples: Blank = No Options

2 - Series-Damping Resistor on Outputs

4 - Level Shifter

25 – 25-Ω Line Driver

7 Function

Examples: 244 - Noninverting Octal Buffer/Driver

374 - Octal D-Type Flip-Flop

573 - D-Type Transparent Latch

640 - Inverting Octal Transceiver

8 Device Revision

Examples: Blank = No Revision

Letter Designator A-Z

9 Packages

Examples: D, DW - Small-Outline Integrated Circuit (SOIC)

DB, DBQ, DL - Shrink Small-Outline Package (SSOP)

DBB, DGV - Thin Very Small-Outline Package (TVSOP)

DBV, DCK - Small-Outline Transistor Package (SOT)

DGG, PW - Thin Shrink Small-Outline Package (TSSOP)

FK - Leadless Ceramic Chip Carrier (LCCC)

FN – Plastic Leaded Chip Carrier (PLCC) GB – Ceramic Pin Grid Array (CPGA)

HFP, HS, HT, HV – Ceramic Quad Flat Package (CQFP)

J. JT – Ceramic Dual-In-Line Package (CDIP)

N, NP, NT – Plastic Dual-In-Line Package (CDIP)

PAG. PAH. PCA. PCB. PM. PN. PZ -

Plastic Thin Quad Flat Package (TQFP)

PH. PQ. RC – Plastic Quad Flat Package (QFP)

W, WA, WD – Ceramic Flat Package (CFP)

10 Tape and Reel

Examples: Blank - Not Taped and Reeled

R - Reeled Product†

† All reeled material previously designated LE continues to be reeled left embossed, but an R designator is used.



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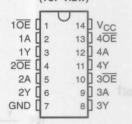
SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS703C - AUGUST 1997 - REVISED MAY 1998

 State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation

- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

SN54LVTH125...J PACKAGE SN74LVTH125...D, DB, OR PW PACKAGE (TOP VIEW)



SN54LVTH125 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

description

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH125 devices feature independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (\overline{OE}) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH125 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH125 is characterized for operation from –40°C to 85°C.

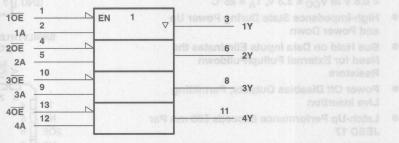


SCBS703C - AUGUST 1997 - REVISED MAY 1998

FUNCTION TABLE (each buffer)

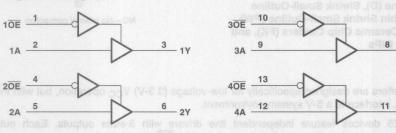
INPL	JTS	OUTPUT
OE	Α	Υ
L	Н	VH) o
L	L	Vab)
Н	X	Zno

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, and PW packages.

logic diagram (positive logic)



8 3Y

Pin numbers shown are for the D, DB, J, and PW packages.

SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS703C - AUGUST 1997 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, Vcc	
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-in	
	ate, V _O (see Note 1)0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, Io: SN54	LVTH125 96 mA
	4LVTH125 128 mA
Current into any output in the high state, IO (see	Note 2): SN54LVTH125 48 mA
	SN74LVTH125 64 mA
Input clamp current, IIK (VI < 0)	
Output clamp current, IOK (VO < 0)	
) package 127°C/W
0.5	OB package
88.0 F	PW package 170°C/W

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

Aar 1			V E = QV	SN54LV	TH125	SN74LV	TH125	LINUT
				MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		O=0.6 V to 3 V.	2.7	3.6	2.7	3.6	V
VIH	High-level input voltage			2	100 3	2		٧
VIL	Low-level input voltage		O=05V103V	W.DolVa.	0.8		0.8	V
VI	Input voltage			918371	5.5		5.5	٧
IOH	High-level output current	-51.0	Outputs high	1 6	-24	1	-32	mA
loL	Low-level output current		West Riscond	3	48		64	mA
Δt/Δv	Input transition rise or fall rate	e *****	Outputs enabled	0	10	1	10	ns/V
Δt/ΔVCC	Power-up ramp rate		A 9.0 - 30 A IR YOU BUILD	200	F = 50)	200		μs/V
TA	Operating free-air temperatur	re .		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS SCBS703C - AUGUST 1997 - REVISED MAY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

V C mai		TEOT 0	ONDITIONS	SNS	54LVTH	125	SN7	74LVTH1	25	HAUT	
PAI	RAMETER	IESI C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
VIK	/ 3.0	V _{CC} = 2.7 V,	I _I = -18 mA	1	t etek	-1.2	late. V.	à flo-ne	-1.2	V	
18.0+	0.5 V to Vcc	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0	2	o yns o	VCC-0.	2	es age	loV	
98 m/		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	ME WO	n ine l	2.4	to any	ni iner	V	
VOH		V 0.V	I _{OH} = -24 mA	2						V	
		VCC = 3 V	I _{OH} = -32 mA	sh Or tare	ns ugu	i em n	2	to any	HI HIST	UD :	
km Da-		V _{CC} = 2.7 V	I _{OL} = 100 μA		- 1	0.2	and down	and the last	0.2	mail	
		VCC = 2.7 V	I _{OL} = 24 mA		10 -	0.5	d toes	HO CIRCU	0.5		
Vol.			I _{OL} = 16 mA	e Note 3	es) ALG	0.4	seconi l	amed	0.4	V	
		V 2V	I _{OL} = 32 mA			0.5			0.5	V	
		VCC = 3 V	I _{OL} = 48 mA			0.55	1 500				
		and the second	I _{OL} = 64 mA	= 64 mA				ampera	0.55	Sto	
na ylno	are stress mlings	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	atinbecau	mixem d	10	sebnu be	tell scori	10	Bazaet	
on si "an II .bei	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Name and	o you	989±1	edivide	on of the	±1	μА	
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}	enter erreiting		1	n transfern I	ora hvid	1	μΛ	
	Data Inputs	vCC = 3.0 v	VI = 0 OV boa etste dol	d and milet	\$10.01	-5	rina swol	t Inemus	-5		
loff		$V_{CC} = 0$,	V_{1} or $V_{0} = 0$ to 4.5 V	e betalig) a 2i 80	mpedan	lamed	package	±100	μΑ	
lea en	Data inputs	V _{CC} = 3 V	V _I = 0.8 V	75			75			μА	
II(hold)	Data inputs	ACC = 2 A	V _I = 2 V	-75			-75			μм	
IOZH	SN74LVTH125	V _{CC} = 3.6 V,	V _O = 3 V			5			5	μΑ	
lozL	XAM MIN	V _{CC} = 3.6 V,	V _O = 0.5 V			-5			-5	μΑ	
lozpu	2.7 3.6	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	0.5 V to 3 V,			±50*	et out voice		±50	μА	
lozpd		$\frac{V_{CC}}{OE}$ = 1.5 V to 0, V_{O} =	0.5 V to 3 V,			±50*	garlov jur	pri level-	±50	μА	
Am	66-	VCC = 3.6 V,	Outputs high		0.12	0.19	core tomb	0.12	0.19	i lar	
Icc		$I_{O} = 0$,	Outputs low	a laws	4.5	7	ero its fallen	4.5	7	mA	
Man	101	V _I = V _{CC} or GND	Outputs disabled	The Lorent	0.12	0.19	n ash no	0.12	0.19	1 1455	
ΔI _{CC} ‡	200	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND				0.3	elin qu	un qui ra	0.2	mA	
Ci		V _I = 3 V or 0			4	910/10/19/1		4	990	pF	
Co	assemble to land or	V _O = 3 V or 0	PUNE CLO CHAIN IN SOLD	1	8	Columbia	CA CA TOWN	8	Personal Personal	pF	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

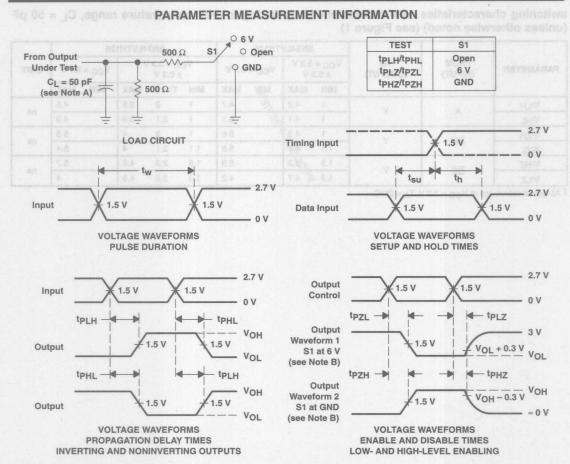
SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS703C - AUGUST 1997 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	LS .	TO (OUTPUT)	SN54LVTH125				SN74LVTH125						
	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
t _{PLH}	A	V	1	4.2	4	4.7	1	2	3.5		4.5		
t _{PHL}		^	1	1	4.1	0-	5.1	1	2.1	3.9	+	4.9	ns
^t PZH	- V	V	1	4.9	2	5.6	1	2	4		5.5		
tPZL	OE	OE I	T	1.1	4.9		5.6	1.1	2.1	4		5.4	ns
tPHZ	14 OF 14	OF V		6.3		5.9	1.5	2.3	4.5	- Maria	5.7	no	
tPLZ	OE	UE I	1.3	Q 4.7		4.2	1.3	2.8	4.5		4	ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



NOTES: A. CL includes probe and jig capacitance.

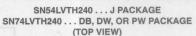
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH240, SN74LVTH240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

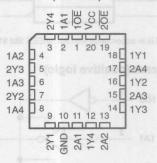
SCBS679C - DECEMBER 1996 - REVISED MARCH 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V **Operation and Low Static Power** Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V VCC)
- **Support Unregulated Battery Operation** Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- **Power Off Disables Outputs, Permitting** Live Insertion
- **Bus Hold on Data Inputs Eliminates the** Need for External Pullup/Pulldown
- Latch-Up Performance Exceeds 500 mA JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- **Package Options Include Plastic** Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs





SN54LVTH240 . . . FK PACKAGE (TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are organized as two 4-bit buffer/line drivers with separate output-enable (OE) inputs. When OE is low, the devices pass data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

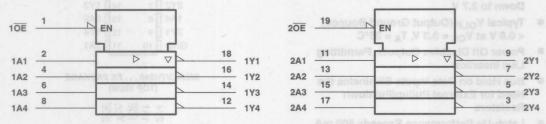
The SN54LVTH240 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVTH240 is characterized for operation from -40°C to 85°C.

SCBS679C - DECEMBER 1996 - REVISED MARCH 1998

FUNCTION TABLE (each buffer)

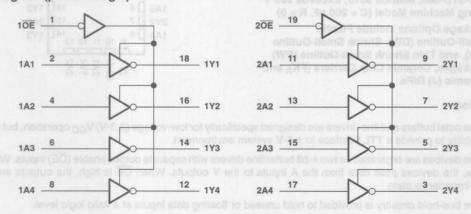
INP	JTS	OUTPUT
OE	Α	Y
L	Н	Lot
L	L	Н
Н	X	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCBS679C - DECEMBER 1996 - REVISED MARCH 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, Voc		
Voltage range applied to any output in		
or power-off state, Vo (see Note 1)		0.5 V to 7 V
Voltage range applied to any output in	the high state, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
	e, IO: SN54LVTH240	
V. Comments	SN74LVTH240	
Current into any output in the high sta	te, IO (see Note 2): SN54LVTH240	48 mA
	SN74LVTH240	64 mA
Input clamp current, I _{IK} (V _I < 0)	Au 007 = 101	
Output clamp current, IOK (VO < 0) .	Am F2 = 101	–50 mA
	e Note 3): DB package	
0.5	DW package	
	PW package	128°C/W
Storage temperature range, T _{stg}		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVT	H240	SN74LV	TH240	LINUT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	VEOLVEO	2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	4	2		V
VIL	Low-level input voltage	O = 0.6 V to 3 V,	V DOLVET	0.8		0.8	٧
VI	Input voltage	1	8 BD 10 Q	5.5		5.5	V
ЮН	High-level output current	Real studies C	VA	-24		-32	mA
loL	Low-level output current	Well steated	3	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	0	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	Value SQV is tuggi sec	2 200	Yes	200		μs/V
TA	Operating free-air temperature	White He	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN54LVTH240, SN74LVTH240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS679C - DECEMBER 1996 - REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

/ T of 1/	2.0			SN	54LVTH	240	SN	74LVTH2	240	ni
PAI	RAMETER	TEST	CONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNI
VIK	2.0-	V _{CC} = 2.7 V,	I _I = -18 mA	(Note	-1.2	V.,etati	tlo-19	-1.2	V
+ 0,5	0.5 V to V.c.	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0	.2	o any o	VCC-0	2 000	itage n	oV.
VoH		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	ers wor	ent or	2.4	no any	n men	V
		V 01/	I _{OH} = -24 mA	2						V
		V _{CC} = 3 V	I _{OH} = -32 mA	TO LOW	PS. TAPUT	QUI IN	2	ALIE ON	2.3536211	
Am 08-		V 07V	I _{OL} = 100 μA	0.2			out tous	nus ae	0.2	int
		V _{CC} = 2.7 V	I _{OL} = 24 mA		10.57	0.5	0.5			
,o ar			I _{OL} = 16 mA	acold as	8 ta 180	0.4	ecomi li	therms	0.4	V
VOL		V 0V	I _{OL} = 32 mA			0.5		305	0.5	V
		VCC = 3 V	I _{OL} = 48 mA			0.55				
			I _{OL} = 64 mA		er gle	1,000	emperature ra		0.55	18
ta yino s	gridan sagrus em	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	in illes mu	ribaism ed	10	statu bol	those ils	brio 10	(ARED)
li Li	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	lb taa well	NI BOX	±1	DOMEND IS	rtt lo nor	±1	цА
	Data inputs	Vcc = 3.6 V	V _I = V _{CC}	testage est	S	1	distribution in	ens heari	1	μА
	Data Inputs	ACC = 2.0 A	V _I = 0 0 v boo state don	Leatrof all	my or	-5	thouse on	memup.	-5	
loff		$V_{CC} = 0$,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5 \text{ V}$	rifpelslip	5	(Ubisolini	senedi	parting	±100	μΑ
I _I (hold) Data inputs		V _{CC} = 3 V	V _I = 0.8 V	75	No. of Street		75			μА
I(hold)	Data Inputs	ACC = 2 A	V _I = 2 V	-75			-75			μΛ
lozh	GESTET KANTON	$V_{CC} = 3.6 V,$	V _O = 3 V			5			5	μА
lozL	XAM HIM	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V			-5			-5	μА
lozpu		$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	= 0.5 V to 3 V,			±100*	sikay jug		±100	μА
OZPD	5.8	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = \frac{V_{CC}}{OE} = \frac{1.5 \text{ V to 0, V}_{O}}{OE} = 1.$	= 0.5 V to 3 V,			±100*	alloy ha	ri levati spellov ti	±100	μА
Am	98-1-	V _{CC} = 3.6 V,	Outputs high			0.19	cue bichi	n lavete	0.19	140
loc		I _O = 0,	Outputs low			5	our nich	io laval-	5	m/
Vlan	07	V _I = V _{CC} or GND	Outputs disabled			0.19	n extrato	than out h	0.19	
Δlcc [‡]	603	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND				0.2	eser cim	an openin	0.2	mA
Ci	mallana IT and	V _I = 3 V or 0		a libraria	3		Total Control	3	ALAMA II A	pF
Co		V _O = 3 V or 0	1001/202 sections	ne official	7	T excite of	H MAN SHARE	7	bardored	pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

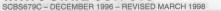
SN54LVTH240, SN74LVTH240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

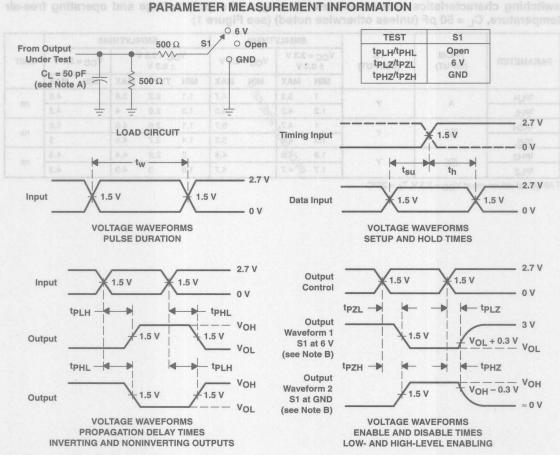
SCBS679C - DECEMBER 1996 - REVISED MARCH 1998

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_1 = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER		NPUT) (OUTPUT)	SN54LVTH240				SN74LVTH240						
	FROM (INPUT)			V _{CC} =	3.3 V 3 V	Vcc=	2.7 V	V	cc = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
	GND		MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
t _{PLH}	А	Y	1	3.9	20	4.7	1.1	2.2	3.8		4.6	ns	
t _{PHL}			Ť	1.2	4.2	44	4.3	1.3	2.6	4	=	4.2	115
t _{PZH}	75	Y	1	4.7	Q.	5.7	1.1	2.6	4.6		5.6	200	
tPZL	ŌĒ	1	1.3	4.6		5.2	1.4	2.7	4.4		5	ns	
tPHZ	ŌĒ	Y	1.9	4.6		4.8	2	2.9	4.4	Nation 1	4.6	no	
tPLZ	OE	re ²	1.7	2 4.7		4.7	1.8	3	4.3		4.3	ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.





NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Q} = 50 Ω , $t_{f} \leq$ 2.5 ns. $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

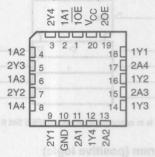
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH241, SN74LVTH241 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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	State-of-the-Art Advanced BiCMOS			SN54LVTH241 J PACKAGE				
	Technology (ABT) Design for 3.3-V		SN7		DW, OR PW PACKAGE			
	Operation and Low Static Power			(TOP VIEW)				
0.00	Dissipation			10E [1	20 VCC			
•	High-Impedance State During Power	r Up		1A1 2	19 20E			
	and Power Down			2Y4 🛚 3	18 1Y1			
	 Support Mixed-Mode Signal Operation 			1A2 [4	17 2A4			
	(5-V Input and Output Voltages With			2Y3 🛮 5	16 1Y2			
	3.3-V V _{CC})			1A3 [6	15 2A3			
	Support Unregulated Battery Operat	tion		2Y2 🛮 7	14 1Y3			
	Down to 2.7 V			1A4 🛮 8	13 2A2			
	Typical V _{OLP} (Output Ground Bound	ce)		2Y1 🛮 9	12 1Y4			
	< 0.8 V at V _{CC} = 3.3 V, T _A = 25°C	,,		GND [10	11 2A1			
•	Power Off Disables Outputs, Permitt Live Insertion	ting		SN54LVTH241.	FK PACKAGE			

(TOP VIEW)



Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors

 Latch-Up Performance Exceeds 500 mA Per JESD 17

ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

description

These octal buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH241 devices are organized as two 4-bit line drivers with separate output-enable (10E, 20E) inputs. When $1\overline{OE}$ is low or $2\overline{OE}$ is high, the devices pass noninverted data from the A inputs to the Y outputs. When 10E is high or 20E is low, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54LVTH241 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVTH241 is characterized for operation from -40°C to 85°C.



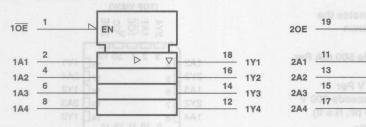
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FUNCTION TABLES

INPL	JTS	OUTPUT
10E	1A	1Y
L	Н	Н
L	L	LqU
Н	X	Z

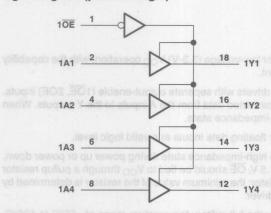
INP	JTS	OUTPUT
20E	2A	2Y
Н	Н	Н
Н	L	L
L	X	Z

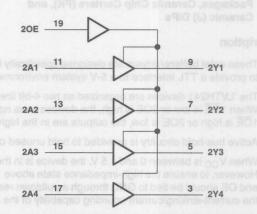
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





EN

D

 ∇

9

7

3

5

2Y2

2Y3

2Y4

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
	2	
Voltage range applied to any output in		
or power-off state, Vo (see Note 1)		0.5 V to 7 V
Voltage range applied to any output in	the high state, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Current into any output in the low state	e, I _O : SN54LVTH241	96 mA
V	SN74LVTH241	
Current into any output in the high sta	te, IO (see Note 2): SN54LVTH241	48 mA
	SN74LVTH241	64 mA
Input clamp current, IIK (VI < 0)	Au 001 = 101	
Output clamp current, IOK (VO < 0) .	Am 42 = jol	
	e Note 3): DB package	
0.6	DW package	97°C/W
	PW package	
Storage temperature range, Tstg		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

Au la	Te Te	V6=0V	SN54LVTH241	SN74LVTH241	UNIT
			MIN MAX	MIN MAX	
Vcc	Supply voltage	V S of V B O = OV	2.7 3.6	2.7 3.6	V
VIH	High-level input voltage	61	150 230 3	2	V
VIL	Low-level input voltage	VO = 0.5 V to 3 V.	8.0 - 1.5 VIO	0.8	V
VI	Input voltage	9	5.5	5.5	٧
ЮН	High-level output current	Outputs high	-24	-32	mA
loL	Low-level output current	** Outputs low	3 48	64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	0 10	10	ns/V
Δt/ΔVCC	Power-up ramp rate	7 S.O - 50V is highl end 3	2 200	200	μs/V
TA	Operating free-air temperature		-55 125	-40 85	°C

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN54LVTH241, SN74LVTH241 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Valor 7	P.A.		OVERTIONS	SNS	54LVTH2	241	SN7	74LVTH2	41	W.	
PAI	RAMETER	TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
VIK	-0.5	V _{CC} = 2.7 V,	I _I = -18 mA		Note	-1.2	V ,sink	ito-ne	-1.2	V	
3.0+5	-0.5 V to Voc	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0	2	o any o	VCC-0.	2	n agasti	DV	
. 96 m		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	ata wo	901.10	2.4	Aus ca	I TERM	V	
VOH		V 0V	I _{OH} = -24 mA	2						V	
		V _{CC} = 3 V	I _{OH} = -32 mA	Or series	P. INI	N 1 1 1 1	2	tilo em	N ALICAN		
m 0a-		V 0.7.V	I _{OL} = 100 μA		R	0.2	and Arrive	burn cia	0.2	ini	
		V _{CC} = 2.7 V	I _{OL} = 24 mA		10.27	0.5	friend	n eme	0.5		
sorarr			I _{OL} = 16 mA	se Note:	a) a) O	0.4	eam k	therms	0.4	19	
VOL		V 0V	I _{OL} = 32 mA		0.5					V	
		VCC = 3 V	I _{OL} = 48 mA		0.55						
			I _{OL} = 64 mA		· · · pre	nge, L	n anols	neqma	0.55		
na vino ar	atter seeviness e	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	eg tiben mun	nazin	10	elonu beh	those the	10	раветя	
lı	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	to too leafit	YOU TE	±1	BOIVED IS	ra no	±1	riollars.	
	Data insula	V 0.6V	V _I = V _{CC}	ser sionital	B.	1	Supplied la	da teani	1	μΑ	
Data inputs		V _{CC} = 3.6 V	V _I = 0	tartini ai b	to the state of ree-5			Inequa:	-5		
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V	a sterior Sil son sociali		annert e	Bankasa.	±100	μА		
lan an	Data innuta	V 2V	V _I = 0.8 V	75) - (A)		75	one be	to second		
II(hold)	Data inputs	VCC = 3 V	V _I = 2 V	-75	NA STATE OF		-75			μА	
lozh	BRYALVINZET	V _{CC} = 3.6 V,	V _O = 3 V			5			5	μА	
lozL	XAM VISI	V _{CC} = 3.6 V,	V _O = 0.5 V			-5			-5	μА	
lozpu	2 2	$\frac{V_{CC}}{OE/OE} = 0$ to 1.5 V, $V_{O} = 0$	0.5 V to 3 V,			±100*	go gut voite	allov ydda h-teval ir	±100	μА	
IOZPD	8.0	$\frac{V_{CC}}{OE/OE} = 1.5 \text{ V to 0, V}_{O} = \frac{1.5 \text{ V to 0, V}_{O}}{OE/OE} = \frac{1.5 \text{ V to 0, V}_{O}}{OE/O$	= 0.5 V to 3 V,			±100*	afkov tyg	orloval v	±100	μА	
Asn	SE-		Outputs high			0.19	nas faran	o lineal-ri	0.19	NO	
lcc		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs low			5	tuo heth	na lavatie	5	mA	
		1-1000000	Outputs disabled	1		0.19	o outrain	Demost to	0.19		
Δlcc [‡]	200	V _{CC} = 3 V to 3.6 V, On Other inputs at V _{CC} or	e input at V _{CC} – 0.6 V, GND			0.2	etar omi	a dn-len	0.2	mA	
Ci	TV sale is	V _I = 3 V or 0			3			3	a from a M.C.	pF	
Co		V _O = 3 V or 0	ERORAGOR SICRADOR	na logil school	7	Laurante de	a formalis	7	Managara .	pF	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested. † All typical values are at V $_{\rm CC}$ = 3.3 V, T $_{\rm A}$ = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVTH241, SN74LVTH241 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

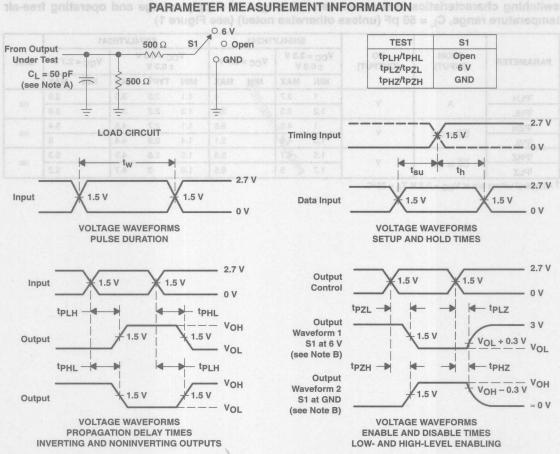
	ra l	TO (OUTPUT)		SN54L\	/TH241	0.0	SN74LVTH241					
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
	ONE		MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
t _{PLH}	^		1	3.7	14	4	1.1	2.3	3.5		3.9	-
tPHL	Α	T	1.2	3.5	54	3.7	1.3	2.2	3.4		3.6	ns
t _{PZH}	- OF	V	1	4.6	3	5.5	1.1	2.7	4.5		5.4	
tPZL	OE or OE	T	1.3	4.6		5.1	1.4	2.9	4.4		5	ns
t _{PHZ}	<u> </u>	V	1.5	4.7		5.5	1.6	2.8	4.5		5.3	200
tPLZ	OE or OE	7	1.7	2 5		5.5	1.8	3	4.7		5.2	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

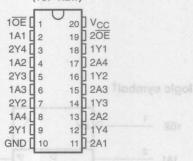
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

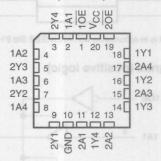
SCAS586C - DECEMBER 1996 - REVISED MARCH 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Power Off Disables Outputs, Permitting Live Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVTH244A . . . J OR W PACKAGE SN74LVTH244A . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTH244A . . . FK PACKAGE (TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH244A devices are organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

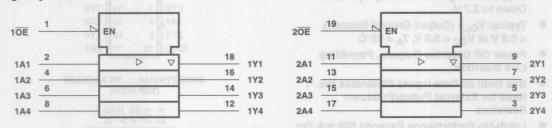
The SN54LVTH244A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH244A is characterized for operation from –40°C to 85°C.



FUNCTION TABLE (each buffer)

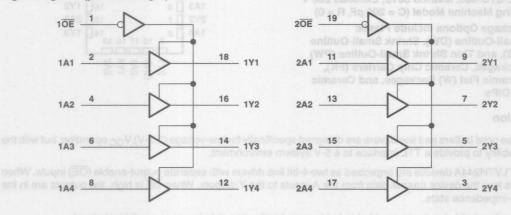
INP	JTS	OUTPUT
OE	Α	Y
L	Н	Hat
L	L	L
Н	X	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to 4.6 V Input voltage range, V _I (see Note 1)0.5 V to 7 V Voltage range applied to any output in the high-impedance
or power-off state, V _O (see Note 1)
Voltage range applied to any output in the high state, V _O (see Note 1)—0.5 V to V _{CC} + 0.5 V Current into any output in the low state, I _O : SN54LVTH244A96 mA SN74LVTH244A
Current into any output in the high state, I _O (see Note 2): SN54LVTH244A
$ \begin{array}{llllllllllllllllllllllllllllllllllll$
Package thermal impedance, θ _{JA} (see Note 3): DB package
DW package
Storage temperature range, T _{stg} 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

Au S		V 8 = DV	SN54LVT	H244A	SN74LVT	UNIT	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	V.E of V.E.o.	2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	nob = 3	2		V
VIL	Low-level input voltage	V 8 of V 8.0	WHO OF WO	0.8	1	0.8	V
VI	Input voltage		97807	5.5		5.5	V
ЮН	High-level output current	Outputs high	VE	-24	/	-32	mA
loL	Low-level output current	Well employ 1		48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	OF ILLES	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	v a.0 – 0.0 V to lugar a	200	E = 00	200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCASS86C - DECEMBER 1996 - REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

/TotW		7507.0	CAUDITIONIC	SN5	4LVTH2	44A	SN7	4LVTH2	44A	ed
PAI	RAMETER	TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNI
VIK	-0.5	V _{CC} = 2.7 V,	I _I = −18 mA	(1	Note	-1.2	V etsk	tho-ver	-1.2	V
+ 0.5	OD V of V & O-	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0.	2	o sny	VCC-0	2	n egati	oV
m 89		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	ila wol	BUTU	2.4	VILE ON	ii men	0
VOH		V 0V 5115	I _{OH} = -24 mA	2						V
		VCC = 3 V . AAASHI	I _{OH} = -32 mA	Or tenns	e ngin	CHIII ES	2	VIII CILIY	H SHIZIN	
m 08-		V 07V	I _{OL} = 100 μA		R	0.2	of true	en es pue	0.2	ers!
		V _{CC} = 2.7 V	I _{OL} = 24 mA		(D > r	0.5	toese	in come	0.5	
			I _{OL} = 16 mA	ele Mote	8) as 6	0.4	egni l	therms	0.4	V
Vol. (2018)		V 0.V	I _{OL} = 32 mA			0.5			0.5	V
		VCC = 3 V	I _{OL} = 48 mA			0.55				
			I _{OL} = 64 mA	inge, letg			0.55			8
e ylnos	gritar esarté aux	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	illisa mun	nixam el	10	som bei	ell essorti	10	08861
in al "enc II	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	100 12/16	VIIS TO	±1	e device	nt to nor	±1	notion
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}	rations r	acsilev	1	funduo b	oud of the	1.	μА
	Data inputs	VCC = 0.0 V	V _I = 0 DV bne state mark	rif ni ei b	gluc eri	-5	no ewell	Insmuo:	-5	
loff		$V_{CC} = 0$,	V _I or V _O = 0 to 4.5 V	Deladyon	m er son	abaqını.	actieds 6	patoteq	±100	μΑ
len en	A inputs	V _{CC} = 3 V	V _I = 0.8 V	75			75	and had	January 10	μА
I(hold)	Ainputs	ACC = 2 A	V _I = 2 V	-75			-75			μА
lozh	AFRSHTYJETH	V _{CC} = 3.6 V,	V _O = 3 V			5			5	μΑ
IOZL	KAN HIN	$V_{CC} = 3.6 V,$	V _O = 0.5 V			-5			-5	μΑ
lozpu	2.7 3.6	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	0.5 V to 3 V,			±100*	ellov neb	eriov vote nelaval ir	±100	μА
IOZPD	8.0 8.8	V _{CC} = 1.5 V to 0, V _O = OE = don't care	0.5 V to 3 V,			±100*	silos tug	rt leve) o palicy b	±100	μА
Am	1892	V _{CC} = 3.6 V,	Outputs high			0.19	wito Justified	o loval-d	0.19	
lcc		I _O = 0,	Outputs low			5	1900 1000	o Investor	5	mA
		V _I = V _{CC} or GND	Outputs disabled			0.19) aals red	tiensyl h	0.19	
Δlcc‡	200	V _{CC} = 3 V to 3.6 V, One Other inputs at V _{CC} or 0				0.2	etes ami	si qu-ray	0.2	mA
Ci	Constitution of the second	V _I = 3 V or 0			3			3		pF
Co		V _O = 3 V or 0	MODARTIR Salamon mias	and an-ar-	7	Lineline of	A No. of Street	7	a Silveredia	pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS586C - DECEMBER 1996 - REVISED MARCH 1998

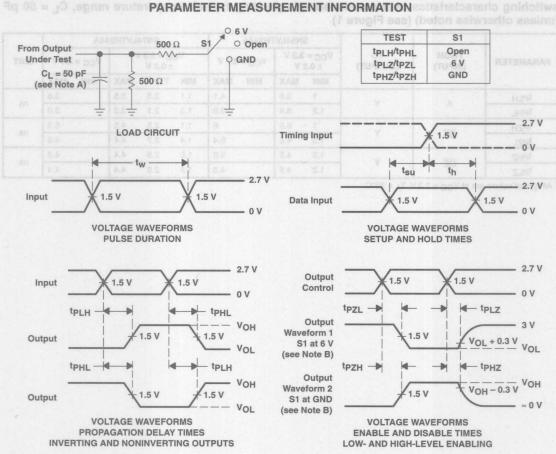
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)		SN54LVTH244A				SN74LVTH244A						
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT		
	GNE		MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX			
^t PLH	А		1	3.6		4.1	1.1	2.3	3.5		3.8	200		
tPHL	^		1.2	3.4		3.9	1.3	2.1	3.3	+	3.6	ns		
^t PZH		V	1	6.9	MEN.	6	1.1	2.5	4.5		5.3			
tPZL	ŌĒ	T	1.3	4.5		5.4	1.4	2.7	4.4		4.9	ns		
t _{PHZ}	- OF	V	1.3	4.5		5.8	1.9	2.8	4.4		4.5	200		
tPLZ	ŌĒ	Y Y	Y	Y	1.2	4.5		4.8	1.8	2.9	4.4		4.4	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



SCAS586C - DECEMBER 1996 - REVISED MARCH 1998



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns,
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS1300 - MAY 1992 - REVISED MARCH 1998

•	State-of-the-Art Advanced BiCMC Technology (ABT) Design for 3.3-		PUNCTIO		154LVTH245A DI		
65	Operation and Low Static Power				(101	VIEW)	
13/10	Dissipation				DIR [1	U 20 VCC	
	High-Impedance State During Po	wer Up			A1 1 2	19 OE	
	and Power Down				A2 3	18 B1	
	Support Mixed-Mode Signal Oper	ration (5-V			A3 [] 4	17 B2	
	Input and Output Voltages With 3	.3-V V _{CC})			A4 🛮 5	16 B3	
	Support Unregulated Battery Ope	eration			A5 [6	15 B4	
	Down to 2.7 V				A6 [7	14 B5	
	Typical V _{OLP} (Output Ground Bo	unce)			A7 [8	13 B6	
	< 0.8 V at V _{CC} = 3.3 V, T _A = 25°C				A8 [9	12 B7	
•	Bus Hold on Data Inputs Elimina Need for External Pullup/Pulldow Resistors				GND [10 SN54LVTH245	11 B8	KAGE
•	Power Off Disables Outputs, Peri	mitting		-45-	A 42 (101)	P VIEW) 또 있旧	
•	Latch-Up Performance Exceeds 5 JESD 17	500 mA Per			3 2	1 20 19	
	ESD Protection Exceeds 2000 V I	Per			A3 4	18	
	MIL-STD-883, Method 3015; Exce	eds 200 V			A4 5	17	
	Using Machine Model (C = 200 pl	R = 0			A5 6	16L	
•	Package Options Include Plastic Small-Outline (DW), Shrink Small	-Outline			A6 7 A7 8 9 10	14 [
	(DB), and Thin Shrink Small-Outl Packages, Ceramic Chip Carriers Ceramic Flat (W) Packages, and	(FK),			A8 GND	B8 B7 B6	ogic diagram (

description

(J) DIPs

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between data buses. They transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH245A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH245A is characterized for operation from –40°C to 85°C.

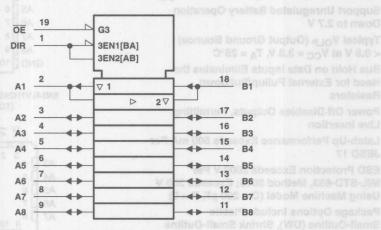


SCBS1300 - MAY 1992 - REVISED MARCH 1998

FUNCTION TABLE

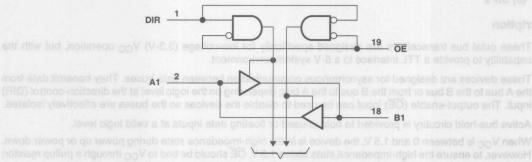
INPUTS	OPERATION	nology (ABT) Design for 3.3 N
DE DIR	OPERATION	nation and Low Static Power
L L	B data to A bus	Ipation
L H	A data to B bus	Impedance State During Por
н х	Isolation	Power Down

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

SCBS1300 - MAY 1992 - REVISED MARCH 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, Vo (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, Io: SN54LVTH245A	
SN74LVTH245A	
Current into any output in the high state, Io (see Note 2): SN54LVTH245A	48 mA
SN74LVTH245A	
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0)	
Package thermal impedance, θ _{JA} (see Note 3): DB package	
DW package	
PW package	128°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

Au	87-	Vie 2 V	SN54LVT	H245A	SN74LVT	H245A	LINUT
		V E of V E D =	MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage	.V s ot V 8,0 €	V 002	8 7 = pp	2		٧
VIL	Low-level input voltage		6,407	0.8	2	0.8	٧
VI	Input voltage	rigirf etuglico	,V4	5.5	1	5.5	٧
ЮН	High-level output current	Wol studied		-24		-32	mA
loL	Low-level output current	Beidesin anglaO	19200714	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	V 8.3 pl)	10	f Con-	10	ns/V
Δt/ΔVCC	Power-up ramp rate	and the second s	200	ogni torii	200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54LVTH245A, SN74LVTH245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS1300 - MAY 1992 - REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

V 0434	3.0	7507	CONDITIONS	SN54LVTH2	45A	SN74L	VTH245A	UNIT	
PAH	RAMETER	TEST	CONDITIONS	MIN TYPT	MAX	MIN 7	TYPT MAX	UNII	
VIK	-0.5	V _{CC} = 2.7 V,	I _I = -18 mA	Note 1)	-1.2	/ state)	-1.2	V	
6.0+	OSV of V a.O-	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$	I _{OH} = -100 μA	V _{CC} -0.2	o any	VCC-0.2	tage range	DV.	
m 80		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	SUL IN	2.4	is out then	V	
VOH		V - 0.V	I _{OH} = -24 mA	2				1 V	
		V _{CC} = 3 V	I _{OH} = -32 mA	S. Service Lifery	COLUMN TO S	2	is one seen	10	
-50 m		V 07V	I _{OL} = 100 μA	- 10	0.2	ul tasan	0.2	and a	
		V _{CC} = 2.7 V	I _{OL} = 24 mA	(0.50	0.5	means	0.5	0	
VOL			I _{OL} = 16 mA	GLA (see Note.	0.4	pamilian	med ap 0.4	V	
		V 0V	I _{OL} = 32 mA		0.5		0.5	7	
		VCC = 3 V	I _{OL} = 48 mA		0.55				
			I _{OL} = 64 mA		,agn	O CHUISH	0.55	115	
na ying a on al "and	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	ute maximuza rapaga	foad±11	Bated unde	georif bnot±1	esant	
	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	Broo tento yna to t	10	solvab etil	10	notion	
h boy	sado ere epolipi	Daumus-grasic lucius br	V _I = 5.5 V	en applica apattov-r	20	todius bris	20	μА	
	A or B ports‡	V _{CC} = 3.6 V	V _I = V _{CC}	the output is in the	necks1	no swell in	musell 1		
			V _I = 0	m berelugisp at son	-5	amied eg	-5		
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V	on all a mallita		- Menne	±100	μΑ	
l	A or B ports	V 2V	V _I = 0.8 V	75		75	A REGION (SER)		
I(hold)	A or B ports	V _{CC} = 3 V	V _I = 2 V	-75		-75		μА	
lozpu	27 3.6	$\frac{V_{CC}}{OE} = 0 \text{ to } 1.5 \text{ V, V}_{O} = 0$	= 0.5 V to 3 V,		±100*	egal	±100	μА	
IOZPD	2 0.6	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = 1.5 \text{ V to 0}$	= 0.5 V to 3 V,		±100*	etlov tugni etlov aucril	±100	μА	
V	8.8	V _{CC} = 3.6 V,	Outputs high		0.19	000	0.19		
loc		I _O = 0,	Outputs low		5	up haduo	avalated 5	mA	
Acr	43	V _I = V _{CC} or GND	Outputs disabled		0.19	nelo hvahim	0.19	10	
ΔICC§	Or Or	V _{CC} = 3 V to 3.6 V, Or Other inputs at V _{CC} or	ne input at V _{CC} - 0.6 V, GND		0.2	eah nollia	0.2	mA	
Ci	=0 02	V _I = 3 V or 0		4	al many		4	pF	
Cio		V _O = 3 V or 0		9			9	pF	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] Unused terminals are at V_{CC} or GND.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SCR\$1300 - MAY 1992 - REVISED MARCH 1998

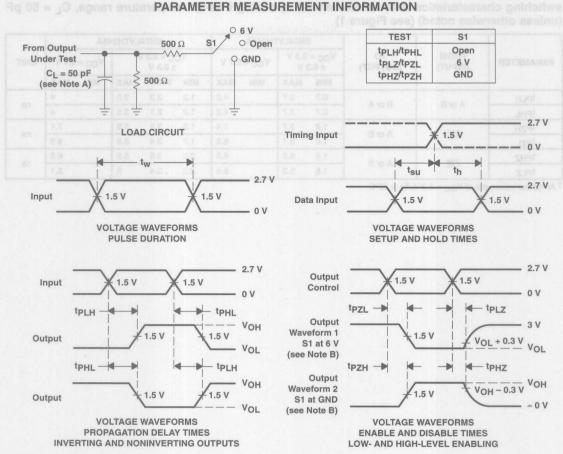
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)	SN54LVTH245A				SN74LVTH245A						
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
t _{PLH}	A or B	B or A	0.7	3.7		4.2	1.2	2.3	3.5		4	no	
tPHL	A or B	BOTA	0.7	3.7		4.2	1.2	2.1	3.5		4	ns	
^t PZH		A == D	1.2	5.7		7.4	1.3	3.2	5.5		7.1		
tPZL	OE	OE A or B	1.6	5.7		6.8	1.7	3.4	5.5		6.5	ns	
tPHZ	PHZ	E A or B	1.8	6.2		6.8	2.2	3.5	5.9	and and	6.5		
tPLZ	ŌĒ		1.8	5.3		5.5	2.2	3.4	5		5.1	ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



SCBS1300 - MAY 1992 - REVISED MARCH 1998



NOTES: A. C_I includes probe and jig capacitance.

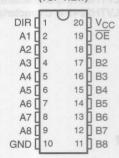
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns,
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

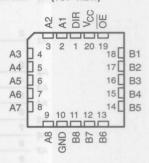
SCRS707B - SEPTEMBER 1997 - REVISED MARCH 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- B-Port Outputs Have Equivalent 22-Ω
 Series Resistors, So No External Resistors
 Are Required
- High-Impedance State During Power Up and Power Down
- Power Off Disables Outputs, Permitting Live Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVTH2245 . . . J OR W PACKAGE SN74LVTH2245 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTH2245 . . . FK PACKAGE (TOP VIEW)



description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between data buses. They transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



SCBS707B - SEPTEMBER 1997 - REVISED MARCH 1998

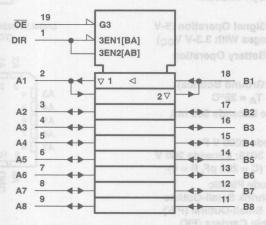
description (continued)

The SN54LVTH2245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH2245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

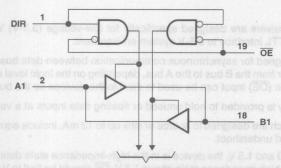
INP	UTS	OPERATION
OE	DE DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
н х		Isolation

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

SCBS707B - SEPTEMBER 1997 - REVISED MARCH 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, Vo (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, Io: SN54LVTH2245 (A port)	96 mA
SN74LVTH2245 (A port)	
B port	30 mA
Current into any output in the high state, IO (see Note 2): SN54LVTH2245 (A port)	
SN74LVTH2245 (A port)	
B port	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Package thermal impedance, θ _{JA} (see Note 3): DB package	
DW package	97°C/W
PW package	
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC. 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

Au 0	ore Control of the Co	V (0.4 of 0 = 6 V to /V	SN54LVTH2245	SN74LVTH2245	UNIT
			MIN MAX	MIN MAX	UNIT
VCC	Supply voltage	V 6 - V	2.7 3.6	2.7 3.6	V
VIH	High-level input voltage	tage Ray and R		2	٧
VIL	Low-level input voltage	\$6.8	0.8	V	
VI	Input voltage	V 6 of V 2.0 =	V 0 al V 0 5.5	5.5	٧
33040	High level autout august	A port	A -24	-32	- A
ЮН	High-level output current	B port	5 -12	-12	mA
Am, è	8 18	A port	8 48	64	200
IOL	Low-level output current	B port	12	12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	V 8 8 01 V 6 = 10	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	CBRD 1	200	200	μs/V
TA	Operating free-air temperature		-55 125	-40 85	°C

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SCBS707B - SEPTEMBER 1997 - REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

7 54 54	3.0	7507.0	ONDITIONS	SN54	LVTH2245	SN	174LVTH2	2245	UNIT	
PAF	RAMETER	TEST C	ONDITIONS	MIN	TYPT MA	X MIN	TYPT	MAX	UNIT	
VIK	2.0-	V _{CC} = 2.7 V,	I _I = -18 mA	(1)	etoVI se=1.	2	a 110-18	-1.2	V	
8.0 +	-0.5 V to Vot	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.2	any outpu	Vcc-	0.2	n sps#	W-	
		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	e wol arti r	2.4	yna oli	ii Inienii	V	
m 881	A port	V 0.V	I _{OH} = -24 mA	2					V	
VOH		VCC = 3 V	I _{OH} = -32 mA		allert all and a	2			and a	
	B port	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$	I _{OH} = -100 μA	V _{CC} -0.2	THERE SHIP I	Vcc-	0.2	p morn	V	
ra DE	Броп	V _{CC} = 3 V,	I _{OH} = -12 mA	2		2		1.12	V	
-50 m		V _{CC} = 2.7 V	I _{OL} = 100 μA		(0 > 0.	2	ATHO CIE	0.2		
	ALESTON AND	vCC = 2.7 v	I _{OL} = 24 mA	Jane 1	0 = 610 0	5	0.5			
	A port		I _{OL} = 16 mA	see Note	A 0 .00 O.	4	thermal	0.4	V	
VOL	Aport	V _{CC} = 3 V	I _{OL} = 32 mA		0.	5		0.5	V	
VOL		ACC = 2 A	I _{OL} = 48 mA		0.5	5				
	0.69-		I _{OL} = 64 mA	A PARTY C	Gist 'ab	ura saum	0.55			
B port	R port	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$	I _{OL} = 100 μA	gritic mumb	omel 20	2	finded list	0.2	V	
	B port	V _{CC} = 3 V,	I _{OL} = 12 mA	OF UP 16/190 Y	J 0.	8	ans to not	0.8	V, I	
bay	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	en ratings me	S ±	1 _n lucituo	orte tugni	err ±1		
	Control inputs	V _{CC} = 0 or 3.6 V,	$V_{ } = 5.5 \text{ V}$	put is in the	A art nert 1	0	Hismus	10		
lj .			V _I = 5.5 V	III JEJISOJOJE	0	edimend	20	μА		
	A or B ports‡	V _{CC} = 3.6 V	VI = VCC	8 0	ialiihaaa	1	and he	1		
		epinion and agree	V _I = 0	- 4	-	5	-5			
loff	CPSARE VAPEN	$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5 V					±100	μΑ	
II(hold)	A or B ports	V _{CC} = 3 V	V _I = 0.8 V	75		75			μА	
'I(HOIG)	/ Or B porto	VCC - 0 V	V _I = 2 V	-75		-75	amino Aidi	drie	pur	
lozpu		$\frac{V_{CC}}{OE} = 0 \text{ to } 1.5 \text{ V}, V_{O} = 0$	0.5 V to 3 V,		±100)*		±100	μА	
lozpd	5.5	$\frac{V_{CC}}{OE}$ = 1.5 V to 0, V_{O} = $\frac{V_{CC}}{OE}$ = don't care	0.5 V to 3 V,		±100)*	egrillov il	±100	μА	
25.01	21-	V _{CC} = 3.6 V,	Outputs high		0.1	9	0.1	0.19	HO	
ICC		I _O = 0,	Outputs low			5	3	5	mA	
Sint	12	V _I = V _{CC} or GND	Outputs disabled		9 0.1 0.19			Jol		
Δlcc§	01	V _{CC} = 3 V to 3.6 V, One Other inputs at V _{CC} or 0			ajst 0.	2	odianent h	0.2	mA	
Ci	A9 04-	V _I = 3 V or 0			4	archit dire-	4	inO.	pF	
Cio	market and the second	V _O = 3 V or 0			9		9		pF	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

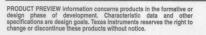
[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ Unused terminals are at V_{CC} or GND.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SCBS707B - SEPTEMBER 1997 - REVISED MARCH 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

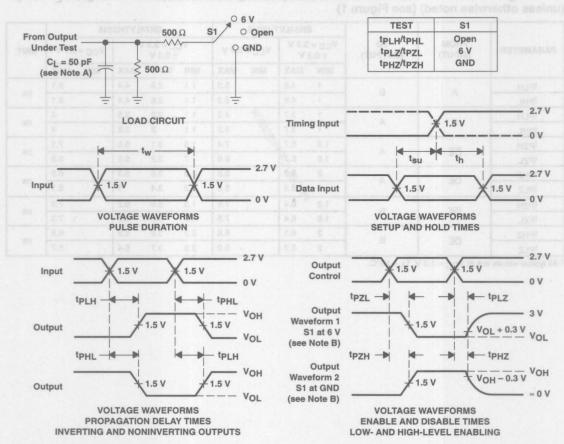
	\$165	TO (OUTPUT)		SN54LV	TH2245	0 1	1 12	SN7	4LVTH2	245			
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V	CC = 3.3 ± 0.3 V	V	V _{CC} =	V _{CC} = 2.7 V		
4			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
tPLH	А	В	-1	4.6		5.3	1.1	2.9	4.4		5.1	ns	
tPHL	^	В	1	4.6		5.3	1.1	2.6	4.4	#	5.1	115	
tPLH	В	A	1	3.7	13	4.2	1.1	2.2	3.5		4		
tPHL	VB.I	^	1	3.7	S	4.2	1.1	2	3.5		4	ns	
^t PZH		A	1.2	5.7	50°	7.4	1.3	3.1	5.5	- ad-	7.1	200	
tPZL	ŌĒ	A	1.6	5.7		6.8	1.7	3.2	5.5		6.5	ns	
tPHZ	ŌĒ	A	2	6,2	W York St	6.8	2.2	3.6	5.9	NUT	6.5		
tpLZ VE	OE	AET X A	2	5.3		5.5	2.2	3.4	5	八八	5.1	ns	
^t PZH		D.	1.2	6.4	400	7.6	1.3	3.5	6.2	-	7.3		
tPZL	OE	BOATABU	1.6	6.4		7.5	1.7	3.7	6.2	VOV	7.3	ns	
tPHZ	OF.	B	2	6.1		6.8	2.2	3.9	5.9		6.5		
tPLZ	ŌĒ	В	2	5.7		5.9	2.2	3.7	5.4	7-11	5.7	ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.





PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCBS136J - MAY 1992 - REVISED APRIL 1998

•	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V		SN74LVTH273 DB, DW, OR PW PACKAGE						
	Operation and Low Static Power Dissipation			CLR (1	7 ₂₀] V _{CC}				
•	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})			1Q [2 1D [3 2D [4	19 8Q 18 8D 17 7D				
•	Support Unregulated Battery Operation Down to 2.7 V			2Q [5 3Q [6	16 7Q 15 6Q				
•	Buffered Clock and Direct Clear Inputs			3D 7 4D 8	14 6D 112 days a 1901				
•	Individual Data Input to Each Flip-Flop Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C			4Q [9 GND [10	12 5Q 11 CLK				
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors			SN54LVTH273.	FK PACKAGE VIEW)				
•	Latch-Up Performance Exceeds 500 mA JESD 17	Per		5 6 6 18	5×8				
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 Using Machine Model (C = 200 pF, R = 0)			2D 4 3 2 1 2Q 5	20 19 18 8D 17 7D				
•	Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW)	1)		3Q 6 3D 7 4D 8	16 7Q 15 6Q 14 6D				
	Packages, Ceramic Chip Carriers (FK), a Ceramic (J) DIPs	ina		0 A Q	50 S				

description

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH273 devices are positive-edge-triggered flip-flops with a direct clear input. Information at the data (D) inputs meeting the setup-time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

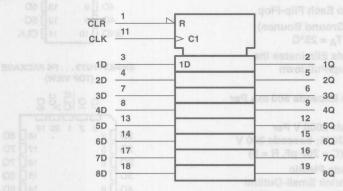
The SN54LVTH273 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVTH273 is characterized for operation from -40°C to 85°C.

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FUNCTION TABLE (each flip-flop)

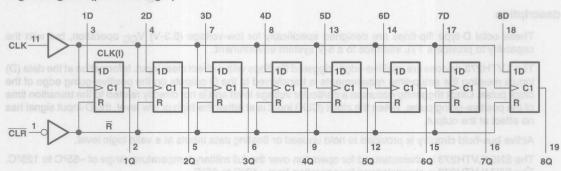
17.0	INPUTS	58 11	OUTPUT
CLR	CLK	D	Q
L	X	X	Loite
Н	1	Н	HIM
Н	1	L	L
Н	HorL	X	Q ₀

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCBS136J - MAY 1992 - REVISED APRIL 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the power-off state, Vo (see Note 1)0.5 V to 7 V
Voltage range applied to any output in the high state, Vo (see Note 1)0.5 V to Vcc + 0.5 V
Current into any output in the low state, IO: SN54LVTH273
SN74LVTH273
Current into any output in the high state, Io (see Note 2): SN54LVTH273
SN74LVTH273 64 mA
Input clamp current, $I_{ K }(V_1 < 0)$
Output clamp current, I _{OK} (V _O < 0)
Package thermal impedance, θ _{JA} (see Note 3): DB package
DW package
PW package
Storage temperature range, T _{stg} 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVTH273	SN74LVTH273	LIMIT
			MIN MAX	MIN MAX	UNIT
Vcc	Supply voltage	NO.	2.7 3.6	2.7 3.6	٧
VIH	High-level input voltage	high by	2 4	2	V
VIL	Low-level input voltage	GMD to	0.8	0.8	V
VI	Input voltage		5.5	5.5	٧
ЮН	High-level output current		<u>0</u> −24	-32	mA
IOL	Low-level output current	or the strain	9 48	64	mA
Δt/Δν	Input transition rise or fall rate	sehrioh	10	10	ns/V
TA	Operating free-air temperature		-55 125	-40 85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

THEV	30		ONDITIONS	SNS	54LVTH2	273	SN	74LVTH2	273	111111111		
PAF	RAMETER	TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT		
VIK	-0.6 V to Voc	V _{CC} = 2.7 V,	$I_{I} = -18 \text{ mA}$	old ordina	luqtuo	-1.2	beilgg	ange a	-1.2	V		
m 89 -		V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0.	2	ent ni	V _{CC} -0.2			0		
VOH		V _{CC} = 2.7 V,	IOH = -8 mA	2.4			2.4			V		
		Van-2V	I _{OH} = -24 mA	2	a ngin	SEL DI	acting.	(I)E ORI	H. JT HOUSE IN	o V		
		V _{CC} = 3 V	I _{OH} = -32 mA		Liv	2						
VoL		v 07V	I _{OL} = 100 μA		10	0.2	10.000	no expens	0.2	-		
		V _{CC} = 2.7 V	I _{OL} = 24 mA	densit aun	el a A	0.5	accei la	semant	0.5			
			I _{OL} = 16 mA			0.4	0.4			V		
		V 2V	I _{OL} = 32 mA			(4) 0.5			0.5	V		
		V _{CC} = 3 V	I _{OL} = 48 mA		14	0.55	n siutaregmel eguito					
		sort a device of or enum	I _{OL} = 64 mA	man este con m	8	doede"	elian/bah	ait neartt	0.55	aneste		
n el feno	Alberoa grittenage	V _{CC} = 0 or 3.6 V,	or 3.6 V, V _I = 5.5 V		900	10	epivab e	iti lo nali	10	nolfanı		
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	THE PERSON C	O DESIGNATION OF THE PARTY OF T	±1	en: cateo	8045, 97, 97	±1	ballqn		
lı bevo	D-1-11-	V 00V	V _I = V _{CC}	and the second second in the				trionsup r	1	μА		
	Data inputs	V _{CC} = 3.6 V	V _I = 0	rii bersiucii	io el ess	-5	emilit i	palasq	-5			
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V						±100	μΑ		
	D-4- it-	V 0 V	V _I = 0.8 V	75	asum	anu i	75	We ha	tyr korr	^		
I(hold)	Data inputs	VCC = 3 V	V _I = 2 V	-75			-75			μА		
lcc	XASK HIM	V _{CC} = 3.6 V, I _O = 0,	Outputs high			0.19			0.19	A		
		V _I = V _{CC} or GND	Outputs low			5		ops/lov	5	mA		
∆lcc‡	$V_{CC} = 3 \text{ V to } 3.6 \text{ V, One}$ Other inputs at V_{CC} or G					0.2	epation.	togal leve bugal lev	0.2	mA		
Ci		V _I = 3 V or 0			4			4	James 1	pF		

[†] All typical values are at VCC = 3.3 V, TA = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		ACTIVATE OF THE PROPERTY OF TH	SN54LVTH273				SN74LVTH273				
	ck Clock frequency		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock				150	The second		Trade of	150			MHz
t _W	Pulse duration		3.3		(3.3		3.3		3.3		ns
	Catum times	Data high or low before CLK↑	2.3	.00	2.7		2.3		2.7		
tsu	Setup time	CLR high before CLK↑	2.3	6,66	2.7		2.3		2.7		ns
th	Hold time, data high or low after CLK↑		0		0	The second	0		0		ns

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAP

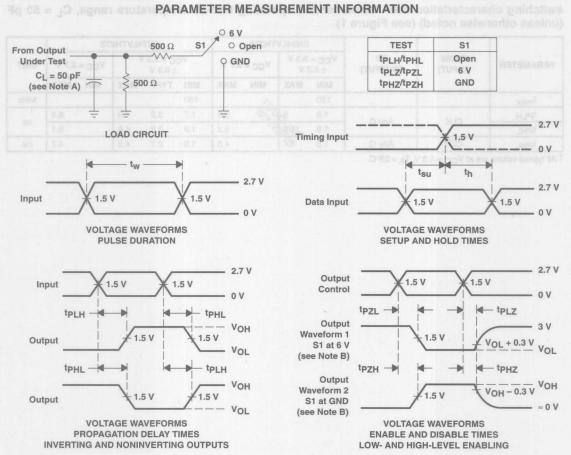
SCBS136J - MAY 1992 - REVISED APRIL 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50 pF$ (unless otherwise noted) (see Figure 1)

PARAMETER	18	Year		SN54L\	/TH273	0 0		SN7	74LVTH2	273		
	FROM TO (OUTPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V	V _{CC} = 2.7 V		UNIT
		HERMETHE	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	100)
fmax			150		4		150					MHz
tPLH	CLK	A	1.6	5	201	5.6	1.7	3.2	4.9		5.5	
t _{PHL}		Any Q	Any Q	1.8	4.9	7,	5.2	1.9	3.2	4.8	a l	5.1
tPHL	CLR	Any Q	1.5	4.4		4.8	1.6	2.7	4.3		4.7	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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NOTES: A. CL includes probe and jig capacitance.

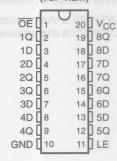
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{Q} = 50 \Omega$, $t_{r} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns,
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

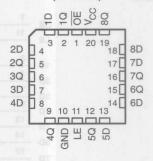
SCBS689D - MAY 1997 - REVISED APRIL 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH373...J OR W PACKAGE SN74LVTH373...DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTH373 . . . FK PACKAGE (TOP VIEW)



description

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



SCBS689D - MAY 1997 - REVISED APRIL 1998

description (continued)

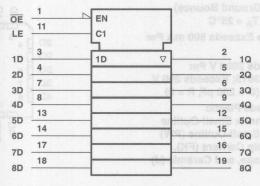
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each latch)

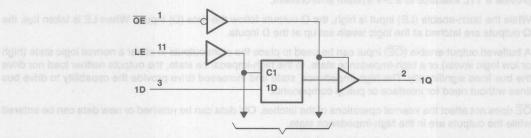
	INPUTS		OUTPUT		
OE	LE D		LE D		Q
L	Н	Н	H		
L	Н	L	L		
L	L	X	Q ₀		
Н	X	X	Z		

logic symbolt



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

SCBS689D - MAY 1997 - REVISED APRIL 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, Vo (see Note 1)	
Current into any output in the low state, Io: SN54LVTH373	96 mA
	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVTH373	
	64 mA
Input clamp current, I _{IK} (V _I < 0)	-50 mA
Output clamp current, I _{OK} (V _O < 0)	
Package thermal impedance, θ,IA (see Note 3): DB package	
	97°C/W
PW package	
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV	TH373	SN74LVTH373		LINUTE
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	V g at V 8.0 = AV	2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage	Etalogue a a partir de la compa	2	4	2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage		1180 71100	5.5		5.5	٧
ЮН	High-level output current	Curbons tubu	Action	-24		-32	mA
loL	Low-level output current	war erugino	0 0 5	48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	0	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	A KAN - DOA'N WALKON A	2 200	00 Y 1	200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

T			ONDITIONS.	SN	54LVTH	373	SN7	4LVTH3	373	LIAUS		
PAI	RAMETER	TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT		
VIK	8.0-	V _{CC} = 2.7 V,	I _I = -18 mA	Siere (Note	-1.2	/ etate	No-ret	-1.2	V		
ā.0 + p	-0.5 V to V _{CC}	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0	.2	yris o	VCC-0.	2 000	lege r	W.		
m 88		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	low siz	en me	2.4	(rus otr	ii Jingmi	0,,		
VOH		V 0V	I _{OH} = -24 mA	2				1111		V		
		VCC = 3 V	I _{OH} = -32 mA	OL'SIS	DE LIGHT	Bull Cit	2	INS CIT	ninem			
m 08-	****	V 07V	I _{OL} = 100 μA			0.2		al to you	0.2	ent :		
		V _{CC} = 2.7 V	I _{OL} = 24 mA		1000	0.5	1 transpar	a ame	0.5			
11510			I _{OL} = 16 mA	atalt as	IRI ALB	0.4	ocmi le	mark	0.4	V		
VOL		V 2V	I _{OL} = 32 mA			0.5		1901	0.5	V		
		VCC = 3 V	I _{OL} = 48 mA			0.55						
			I _{OL} = 64 mA				n enutereque		0.55	18		
na vino na ita anata ata sa Vo		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	outer mile	10		page habit espeli braw 10		10	82251		
ens' is r	Control inputs	l inputs $V_{CC} = 3.6 \text{ V},$	V _I ' = V _{CC} or GND	lbitop terito) YETS 101	±1	edevice	to to mai	±1	пΔ		
Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}	TOTAL STREET	S.	1	The board and output			μА			
	Data inputs	VCC = 3.6 V	V _I = 0 ov one state ngid		of milet back and man -5			no evol trienus eleT -5				
loff		$V_{CC} = 0$,	V_{1} or $V_{0} = 0$ to 4.5 V	ni beistud	5	rebedmi	e merma	packag	±100	μΑ		
lea e n	Data inputs	V2V	V _I = 0.8 V	75	2		75			μА		
I(hold)	Data inputs	V _{CC} = 3 V	V _I = 2 V	-75	-75		-75			μА		
lozh	SNY4LVTHS73	$V_{CC} = 3.6 V,$	V _O = 3 V			5			5	μА		
OZL	XAM HIM	V _{CC} = 3.6 V,	V _O = 0.5 V			-5			-5	μΑ		
lozpu	2.7 3.6	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	= 0.5 V to 3 V,			±100*	and Andreas	iply volta h-teval la	±100	μА		
lozpo	8.0	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = 0.5 \text{ V to 1}$	= 0.5 V to 3 V,			±100*	e flow fug	ni level-	±100	μА		
Am	SE-	0.00	Outputs high		0.011.00	0.19	in the state of th	a lavial-r	0.19	347		
lcc		$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low			5	The Burns	n lagari	5	mA		
When	01	11-400 01 0140	Outputs disabled	-		0.19	n main mai	length b	0.19			
Δlcc [‡]	008	V _{CC} = 3 V to 3.6 V, Or Other inputs at V _{CC} or	ne input at V _{CC} – 0.6 V, GND			+0.2	eta gini	n qu-tey	0.2	mA		
Ci	100	V _I = 3 V or 0			3			3	No.	pF		
Co	examples a surface	V _O = 3 V or 0	NAVA SANTA MANA	TEL CHICH SILE	7	Name and Address	HARRIES	7	District story	pF		

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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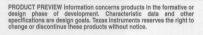
timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54L	VTH373	SN74L		
		V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 2.7 V	UNIT
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t _W	Pulse duration, LE high	3	3	3	3	ns
t _{su}	Setup time, data before LE↓	1.1	0.4	1.1	0.4	ns
th	Hold time, data after LE↓	1.7	2	1.4	1.4	ns

switching characteristics over recommended free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER				SN54L\	/TH373			SN7	74LVTH3	373		
	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V	CC = 3.3 ± 0.3 V	V	Vcc=	2.7 V	UNIT
		VOLTAGE	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
tPLH	D	Q	1.4	4.1		4.7	1.5	2.6	3.9	371	4.5	
t _{PHL}	D	Q	1.4	4.1	1	4.7	1.5	2.6	3.9		4.5	ns
tPLH	TV6	0	1.6	4.4	A V	5.1	1.7	2.7	4.2	//	4.9	
tPHL	V B. J. SLE	LE Q	1.6	4.4	2	5.1	1.7	2.7	4.2	人	4.9	ns
^t PZH	ŌĒ	0	1.2	5		6.1	1.3	3	4.8		5.9	no
tPZL	OE	Q_59	1.2	5		5.7	1.3	3	4.8	AL HI	5.5	ns
tPHZ	ŌĒ	Q	1.8	4.8	H	5.1	1.9	3	4.6		4.9	no
t _{PLZ}	OE	- Q	1.8	4.8	4.0	4.9	1.9	3	4.5		4.6	ns

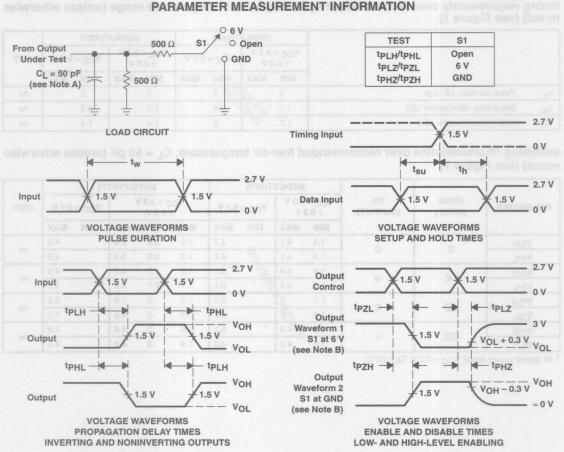
HJ91 - 6 - b





[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.





NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

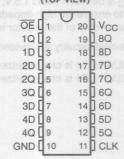
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH374, SN74LVTH374 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

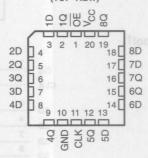
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Power Off Disables Outputs, Permitting Live Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH374...J OR W PACKAGE SN74LVTH374...DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTH374 . . . FK PACKAGE (TOP VIEW)



description

These octal flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVTH374 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54LVTH374, SN74LVTH374 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

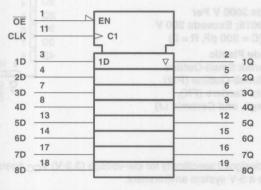
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each flip-flop)

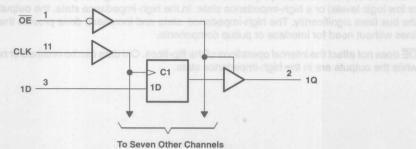
	INPUTS	S	OUTPUT
OE	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	HorL	X	Q ₀
Н	X	X	Z

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH374, SN74LVTH374 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, VO (see Note 1)	
Current into any output in the low state, Io: SN54LVTH374	96 mA
SN74LVTH374	
Current into any output in the high state, IO (see Note 2): SN54LVTH374	
SN74LVTH374	64 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Package thermal impedance, θ _{JA} (see Note 3): DB package	
DW package	97°C/W
PW package	
Storage temperature range, T _{Stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		V 5 = 0V	SN54LV	TH374	SN74LVTH374		CINUT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	VE of V 8.9 = g/V	2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	2	2		٧
VIL	Low-level input voltage	V E or V 8.0 = QV.	Get V d.F.	0.8		0.8	V
VI	Input voltage		PRE- TRUE	5.5		5.5	V
ЮН	High-level output current	agirl singio	Na A	-24		-32	mA
loL	Low-level output current	wol endiers	3	48		64	mA
Δt/Δν	Input transition rise or fall rate	Caldrello sudura 1	20	10	-	10	ns/V
Δt/ΔVCC	Power-up ramp rate	Wild will all the second of th	200	007	200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

T MALE	3.0		ONDITIONS	SNS	4LVTH	374	SN7	74LVTH3	74	UNIT		
PAI	RAMETER	TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT		
VIK	8.0-	V _{CC} = 2.7 V,	I _I = -18 mA	(1	efold	-1.2	Leigh	flo-ter	-1.2	٧		
a.0 + n	-0.6-V to Vo	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0.	2	yns o	VCC-0.	2 3 1 1 3	tage r	W.		
m 88 -		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	ie wol	en) ni	2.4	ms om	i memi	V		
VOH			I _{OH} = -24 mA	2		Cical				V		
		VCC = 3 V	I _{OH} = -32 mA	JF, SIBI	SHORE	DITH IN	2	(THE COST	ringga	Q		
III IPU	****	V 0.7.V	I _{OL} = 100 μA		10	0.2			0.2			
		V _{CC} = 2.7 V	I _{OL} = 24 mA		100	0.5	The Colonia	ex-ruran	0.5			
			I _{OL} = 16 mA	atold so	8 44 (8	0.4	ennile	them.	0.4	V		
VOL WORST OF SE		V 0 V	I _{OL} = 32 mA		0.5				0.5	V		
		VCC = 3 V	I _{OL} = 48 mA	0.55								
			I _{OL} = 64 mA				n e wia	egntai	0.55	8		
na vilno et	oder endste mit na	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	no listas muo	iixaan ed	10	show bots	of electricity	10	585-611		
n ai fanol	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	billion terito	you soy	±1	so visb a	il to noit	±1			
Data inputs	2	VIIIORIII OLIVO	VI = VCC	THE THE COURSE	24	1	CHARLES TO S	DESCRIPTION OF STREET	1	μА		
	Data inputs	V _{CC} = 3.6 V	V _I = 0	t a mini el m	0 A 01	-5	no a non	menuo s	-5			
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V	ra belalicis	5	sbegmi	arro anii e	guidas i	±100	μΑ		
	Data insute	V 0.V	V _I = 0.8 V	750	750° - 76 °		75 -75					
I(hold)	Data inputs	VCC = 3 V	V ₁ = 2 V	-75						μА		
IOZH	FASHUATA URSAY	V _{CC} = 3.6 V,	V _O = 3 V			5		UCY L	5	μΑ		
lozL	KAM NIM	V _{CC} = 3.6 V,	V _O = 0.5 V			-5			-5	μΑ		
lozpu	2.6	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	= 0.5 V to 3 V,			±100*	Fov Juga	diev yleg i laval-d	±100	μА		
lozpd	8.0	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = \frac{V_{CC}}{OE} = \frac{1.5 \text{ V to 0, V}_{O}}{V_{O}} = 1.5 \text{ V to 0,$	= 0.5 V to 3 V,			±100*	ofice/dog	el liporel p	±100	μА		
Am	55-	V _{CC} = 3.6 V,	Outputs high			0.19	and translation	a Javal d	0.19			
Icc		I _O = 0,	Outputs low			5	to real time for		5	mA		
Man		V _I = V _{CC} or GND	Outputs disabled			0.19			0.19			
Δlcc [‡]	200	V _{CC} = 3 V to 3.6 V, On Other inputs at V _{CC} or	e input at V _{CC} - 0.6 V, GND			0.2	also gene	n que rein	0.2	mA		
Ci		V _I = 3 V or 0			3		02 10 00	3	34	pF		
Co	REPORT OF STREET	V _O = 3 V or 0	A STATE OF CHILD AND A STATE OF THE STATE OF	AND AND AND	7	dala ment u	COUNTRION	7	All size year	pF		

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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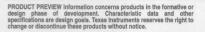
timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	18 1851	SN54LVTH374								
		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		150	4	150		150		150	MHz
t _W	Pulse duration, CLK high or low	3.3	~	3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	1.6	000	2		1.5	anna	2		ns
th	Hold time, data after CLK↑	0.8	6,	0.5		0.8		0		ns

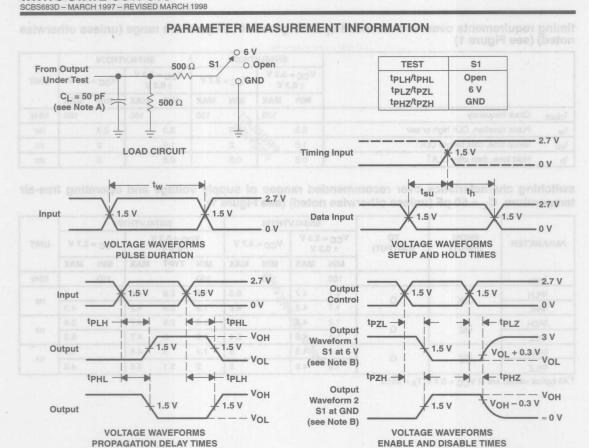
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_{\rm L} = 50$ pF (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)	SN54LVTH374			SN74LVTH374							
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT	
	Samir Gaun C	NR 701124	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
fmax			150		150	2	150			150		MHz	
tPLH	Val	18.F.W.	1.7	4.7	5	5.3	1.8	2.9	4.5	X H	5		
tPHL	CLK	CLK Q	1.7	4.5	SE. A	4.6	1.8	2.9	4.2	- American	4.3	ns	
t _{PZH}	-> 4	Q	1.2	4,9		5.7	1.3	2.8	4.7	THE HUR	5.6		
tPZL	OE	OE I	Q	1.5	4.8	110	5.4	1.6	3	4.7		5.2	ns
tPHZ	WY T YE		1.8	4.8		5	1.9	3	4.6		4.9	0	
tPLZ	ŌĒ	Q	1.9	4.9	-45	5	2	3.1	4.5	1	4.6	ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.







NOTES: A. C_I includes probe and jig capacitance.

INVERTING AND NONINVERTING OUTPUTS

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

LOW- AND HIGH-LEVEL ENABLING

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH540, SN74LVTH540 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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State-of-the-Art Advanced BiCMOS SN54LVTH540 . . . J OR W PACKAGE SN74LVTH540 . . . DB, DW, OR PW PACKAGE Technology (ABT) Design for 3.3-V (TOP VIEW) Operation and Low Static Power Dissipation OE1 20 VCC High-Impedance State During Power Up A1 1 2 19 OE2 and Power Down A2 [3 18 Y1 **Bus Hold on Data Inputs Eliminates the** 17 Y2 A3 1 4 Need for External Pullup/Pulldown A4 16 Y3 Resistors A5 15 Y4 A6 14 Y5 Support Mixed-Mode Signal Operation (5-V A7 13 Y6 Input and Output Voltages With 3.3-V V_{CC}) 8 A8 19 12 Y7 **Support Unregulated Battery Operation** 11 Y8 GND 1 10 Down to 2.7 V Typical VOLP (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V}, T_{A} = 25^{\circ}\text{C}$ SN54LVTH540 . . . FK PACKAGE (TOP VIEW) **Power Off Disables Outputs, Permitting** Live Insertion Latch-Up Performance Exceeds 500 mA Per JESD 17 2 20 19 Y1 **A3** ESD Protection Exceeds 2000 V Per A4 17 MIL-STD-883, Method 3015; Exceeds 200 V A5 Y3 16 Using Machine Model (C = 200 pF, R = 0) A6 15 Y4 **Package Options Include Plastic** A7 Y5 8 Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW)

description

DIPs

These octal buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH540 devices are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH540 is characterized for operation from –40°C to 85°C.

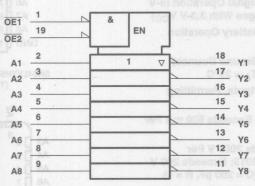


Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) SCBS681D - MARCH 1997 - REVISED MARCH 1998

FUNCTION TABLE

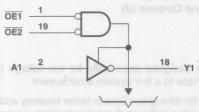
	INPUTS		OUTPUT
OE1	OE2	Α	Y
L	L	L	Н
L	L	Н	SIL 189
Н	X	X	Z
X	Н	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH540, SN74LVTH540 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS681D - MARCH 1997 - REVISED MARCH 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance	
or power-off state, VO (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, Vo (see Note 1)	
Current into any output in the low state, IO: SN54LVTH540	
SN74LVTH540	
Current into any output in the high state, Io (see Note 2): SN54LVTH540	48 mA
SN74LVTH540	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ _{JA} (see Note 3): DB package	
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

Au 8	a	V6=0V	SN54LV	TH540	SN74LVTH540		LINDE
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	V D of V a.0 = OV	2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2	2	2		٧
VIL	Low-level input voltage	V E of V 2.0 = QV .	el V d.I e	0.8		0.8	V
VI	Input voltage		100	5.5		5.5	V
ГОН	High-level output current	High strong	Nox	-24		32	mA
loL	Low-level output current	Computer the second	13	48		64	mA
Δt/Δν	Input transition rise or fall rate	Devinant amount	0	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	ON STATE OF THE ST	200	CONT.	200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

T ALAL				SNS	4LVTH	540	SN	74LVTH5	40	Times.			
PAI	RAMETER	TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT			
VIK	8.0-	V _{CC} = 2.7 V,	I _I = -18 mA		alobi	-1.2	/ lateta	Ro-res	-1.2	V			
8.0 + -	-0.5 V to Vot	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0.	2	Yris o	VCC-0.	.2	tage r	Vo			
m 88 .		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	low st	edt ni	2.4	ros oto	i Insmi	OV			
VOH		V 0.V	I _{OH} = -24 mA	2						V			
		V _{CC} = 3 V	I _{OH} = -32 mA	7-01-9151	a nigin	aut ur	2	ms om	17nem				
III FO		V 0.7.V	I _{OL} = 100 μA	0.2				0.2					
		V _{CC} = 2.7 V	I _{OL} = 24 mA	1 1 1 1 1 1 1	Jan V	0.5	Tenesinal	The second	0.5				
			I _{OL} = 16 mA	atriA on	al as A	0.4	eomi k	arressielt.	0.4	V			
VOL		O.V	I _{OL} = 32 mA			0.5			0.5	V			
		VCC = 3 V	I _{OL} = 48 mA	0.55			1	ALLE L	4.20				
	10 O 0°00		I _{OL} = 64 mA		o pis	I sgn	0.55						
n vino er	oditer anorto era es	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	rielle longe	ixam at	10	about Bas	ellagodti	10	skemi2			
II .	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Direction	WIE HE	¥ ±1	epivib e	rit to noi!	8160±10	function			
		Allikaries especial	V _I = V _{CC}	1			In Style	eds of e	1	μА			
	Data inputs	V _{CC} = 3.6 V	V _I = 0	a di ni si k	1	-5	no awoli	Inento (-5				
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V	mpedance Sucrabequi			amud apaloag a ±100			μА			
	Data laurata	V 0V	V _I = 0.8 V	750	7		75						
I(hold)	Data inputs	V _{CC} = 3 V	V _I = 2 V	-75			-75	μА					
lozh	SMARTATARENO	V _{CC} = 3.6 V,	V _O = 3 V			5			5	μΑ			
lozL	XAM MIN	V _{CC} = 3.6 V,	V _O = 0.5 V			-5			-5	μΑ			
lozpu	2.7 3.6	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	0.5 V to 3 V,			±100*	egi	sply volta	±100	μΑ			
lozpd	8.0	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = \frac{V_{CC}}{OE} = \frac{1.5 \text{ V to 0, V}_{O}}{OE} = 1.$	= 0.5 V to 3 V,			±100*	sflov Jug	ni leval-u	±100	μА			
Am	58	V _{CC} = 3.6 V,	Outputs high	-		0.19		a lawat d	0.19				
ICC		l _O = 0,	Outputs low	-		5		in leave la	5	mA			
		V _I = V _{CC} or GND	Outputs disabled	1		0.19		diament &	0.19				
ΔICC [‡]	200	V _{CC} = 3 V to 3.6 V, On Other inputs at V _{CC} or	e input at V _{CC} - 0.6 V, GND			0.2	elas gras	an qu-taw	0.2	mA			
Ci	CO 04-	V _I = 3 V or 0			3	AMERICA.	0 10 90	3	qu I	pF			
Co	medde is enrorse	V _O = 3 V or 0	nid sing in or ners of 25 A	A DISTRICT	7	BD (50) 10	STUCKED	7	AUTU DA	pF			

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

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[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH540, SN74LVTH540 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS681D - MARCH 1997 - REVISED MARCH 1998

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

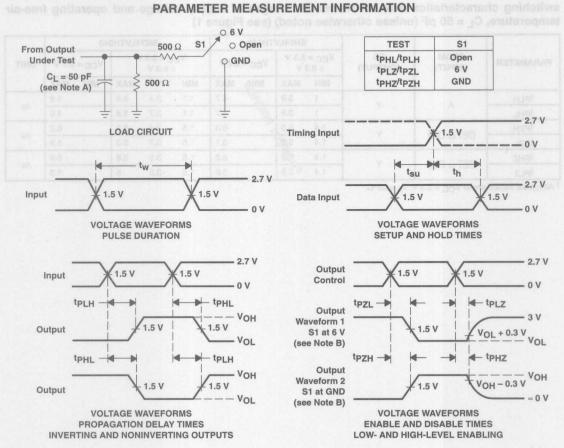
	81	TO (OUTPUT)	SN54LVTH540				SN74LVTH540						
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
t _{PLH}	А		1	3.9	1	4.7	1.1	2.4	3.8		4.6		
t _{PHL}		^	1	1	3.9	24	4.7	1.1	2.7	3.8		4.6	ns
^t PZH	054 050	Y	1.4	5.3	1	6.3	1.5	3.4	5.2		6.2		
tPZL	OE1 or OE2	ı	1.4	5.5	J. Novik	6.1	1.5	3.7	5.3		5.9	ns	
t _{PHZ}	OE4 - OE9	V	1.4	5.9		6.2	1.5	3.9	5.6		5.9	no	
tPLZ	OE1 or OE2	1	1.4	25.5		5.8	1.5	3.5	5	100	5.3	ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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NOTES: A. Cı includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega_s$, $t_f \leq 2.5 \, \text{ns}$, $t_f \leq 2.5 \, \text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

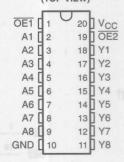
SN54LVTH541, SN74LVTH541 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS682D - MARCH 1997 - REVISED MARCH 1998

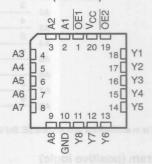
State-of-the-Art Advanced BiCMOS
Technology (ABT) Design for 3.3-V
Operation and Low Static Power
Dissipation

- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Power Off Disables Outputs, Permitting Live Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH541...J OR W PACKAGE SN74LVTH541...DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTH541 . . . FK PACKAGE (TOP VIEW)



description

These octal buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH541 devices are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

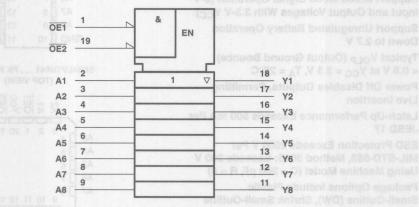
The SN54LVTH541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH541 is characterized for operation from –40°C to 85°C.

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FUNCTION TABLE

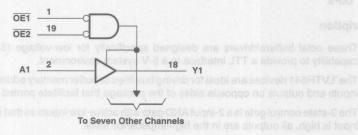
Pilla.	INPUTS	duction.	OUTPUT
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	H H
Н	X	X	Z
X	Н	X	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCBS682D - MARCH 1997 - REVISED MARCH 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

–0.5 V to 4.6 V
0.5 V to 7 V
0.5 V to 7 V
0.5 V to V _{CC} + 0.5 V
96 mA
128 mA
48 mA
64 mA
115°C/W
97°C/W
128°C/W
–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

Au 8		Z V Z V V Z CV			SN74LV	LINUT	
			MIN M	IAX	MIN	MAX	UNIT
Vcc	Supply voltage	V 5 et V 8.0 ≥ 6V l	2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2	12	2		V
VIL	Low-level input voltage	N E of V E.O = OV /	1 1 1 6 1 = CS	0.8		0.8	V
VI	Input voltage		W.	5.5		5.5	V
ЮН	High-level output current	High digitals	3/89-00	-24		-32	mA
loL	Low-level output current	California de la companya de la comp	5	48		64	mA
Δt/Δν	Input transition rise or fall rate	Delease stopuo	0	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	V. One injured VEC 2.6 Vi	200	77	200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN54LVTH541, SN74LVTH541 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

V at A L			0110110110	SNS	4LVTH	541	SN7	4LVTH5	541	LIMIT
PAI	RAMETER	TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	8.0-	V _{CC} = 2.7 V,	I _I = -18 mA	/1	stoi/f	-1.2	/ etate	10-101	-1.2	٧
3.0 + 5	-0.5 V at V _c -	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0.	2	Vr)@ 0	VCC-0.	2	ilage r	1
W 86 .		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	low st	ent ni	2.4	ms ofn	ineru	OV
VOH		V 0V	I _{OH} = -24 mA	2	y Maria					V
		V _{CC} = 3 V	I _{OH} = -32 mA	Tere, Iq.(a ngin	900 DI	2	MB OIN	rinem	
Tradi,	POPPER PROPERTY.	V 07V	I _{OL} = 100 μA		10	0.2			0.2	
		V _{CC} = 2.7 V	I _{OL} = 24 mA	1	10	0.5	in min	n none	0.5	
U UU-			I _{OL} = 16 mA	cinhi na	al and	0.4	un el la	madi	0.4	V
VOL		V 0 V	I _{OL} = 32 mA		The Street	0.5			0.5	V
		VCC = 3 V	I _{OL} = 48 mA			0.55				
			I _{OL} = 64 mA		nta	F,egni	a bure	require.	0.55	
u ulno er	or little bushing data ma	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	odites must	beari an	10	ibnu bas	lisacell	10	Strates
ai Tandi	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	offner conta	yns to	±1	a device	ii to not	±1	^
lı		V 00V	V _I = V _{CC}	TO THE SHAREST	6	1	SATE SAUG	con el el	1	μΑ
	Data inputs	V _{CC} = 3.6 V	V _I = 0	er treit at to		-5	noves on	memuo s	-5	
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V	m perglunii	5	sbegni	armedi è	pulpaq	±100	μΑ
	5		V _I = 0.8 V	750	5		75			
I(hold)	Data inputs	V _{CC} = 3 V	V _I = 2 V	-75	Harris	ALIDO I	-75	qu us	E31101111	μА
lozh	SMINITALY THE 41	V _{CC} = 3.6 V,	V _O = 3 V		N. I.	5			5	μΑ
IOZL	XVIII NIII	V _{CC} = 3.6 V,	V _O = 0.5 V			-5		21.2	-5	μΑ
lozpu	2,7 3.6	V _C C = 0 to 1.5 V, V _O = OE = don't care	= 0.5 V to 3 V,			±100*	age Mov tunn	sply volt.	±100	μА
lozpd	8.0	V _C C = 1.5 V to 0, V _O = OE = don't care	= 0.5 V to 3 V,			±100*	silov hiq	ni level-v	±100	μА
Ann	no.	V _{CC} = 3.6 V,	Outputs high	-		0.19	Lun II and	s I sound of	0.19	
lcc		10 = 0,	Outputs low			5	Land Loren	e buet	5	mA
		V _I = V _{CC} or GND	Outputs disabled			0.19		University for	0.19	
ΔICC [‡]	005	V _{CC} = 3 V to 3.6 V, Or Other inputs at V _{CC} or	ne input at V _{CC} – 0.6 V,			0.2	ater groe	a quetay	0.2	mA
Ci	50 - VI- J	V _I = 3 V or 0			3	NAME OF STREET	67 145-08	3	94	pF
Co	sorajoja (3. sin) 0£19	V _O = 3 V or 0	and emissie at managed 20%	DIEG SQU	7	BQ 8/ 5/ 10	extring to	7	SUPEL I FI	pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH541, SN74LVTH541 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS682D - MARCH 1997 - REVISED MARCH 1998

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_1 = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

7.00	18	TRUT		SN54L\	/TH541	6.3		SN7	4LVTH5	541		mumatit.
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
	оиа	era/ss/ref	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
t _{PLH}	A	Y	1	3.7	30	4	1.1	2.4	3.5		3.9	
t _{PHL}	A	T	1	3.7	200	4	1.1	2.4	3.5		3.9	ns
tPZH	OF OF	Y	1.4	5.3	, a	6.3	1.5	3.5	5.2		6.2	ina
tPZL	OE1 or OE2	T	1.4	5.4		6	1.5	3.7	5.3		5.9	ns
t _{PHZ}	054 050	V	1.4	5.8		6.1	1.5	3.9	5.6		5.9	
tPLZ	OE1 or OE2	Y	1.4	25.4		5.7	1.5	3	5		5.3	ns

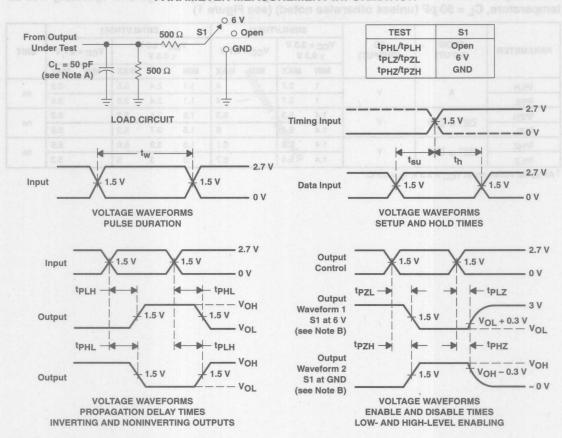
[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.





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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH543, SN74LVTH543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

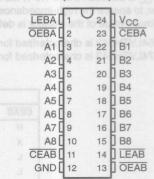
SCBS704C - AUGUST 1997 - BEVISED APRIL 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- **Support Unregulated Battery Operation** Down to 2.7 V
- Power Off Disables Outputs. Permitting Live Insertion
- Typical VOLP (Output Ground Bounce) < 0.8 V at VCC = 3.3 V, TA = 25°C
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883. Method 3015: Exceeds 200 V Using Machine Model (C = 200 pF. R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB). Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages. Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (JT) DIPs

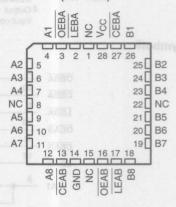
description

These octal transceivers are designed specifically for low-voltage (3.3-V) VCC operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTH543 . . . JT OR W PACKAGE SN74LVTH543 . . . DB, DGV, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTH543 ... FK PACKAGE (TOP VIEW)



NC - No internal connection

The 'LVTH543 devices contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the CEBA, LEBA, and OEBA inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

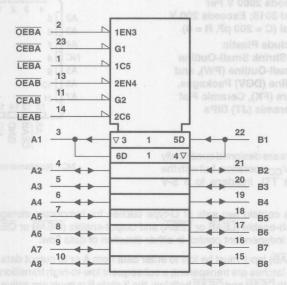
The SN54LVTH543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH543 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

	INPL	JTS		OUTPUT
CEAB	LEAB	OEAB	Α	В
Н	X	X	X	Z
X	X	Н	X	Z
L	Н	L	X	B ₀ ‡
L	L	L	Lac	telm Log
L	L	L	Н	Н

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

logic symbol§

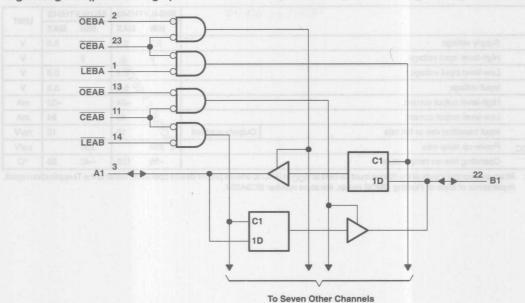


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

[‡]Output level before the indicated steady-state input conditions were established

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logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} 0.5 V to 4.6 V Input voltage range, V_{I} (see Note 1)0.5 V to 7 V Voltage range applied to any output in the high-impedance
or power-off state, V _O (see Note 1)
Voltage range applied to any output in the high state, Vo (see Note 1)0.5 V to Vcc + 0.5 V
Current into any output in the low state, Io: SN54LVTH543
SN74LVTH543
Current into any output in the high state, I _O (see Note 2): SN54LVTH543 48 mA
SN74LVTH543
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0)
Package thermal impedance, θ_{JA} (see Note 3): DB package
DGV package
DW package
PW package
Storage temperature range, T _{stg}

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and VO > VCC.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



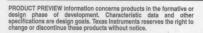
SN54LVTH543, SN74LVTH543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LV	TH543	SN74LV	TH543	111117
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	4	2		V
VIL	Low-level input voltage		, P	0.8	LEBA	0.8	٧
VI	Input voltage			5.5	mann	5.5	٧
ЮН	High-level output current		L	-24		-32	mA
loL	Low-level output current		39	48	DARD	64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	0	10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	·	2 200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.





SN54LVTH543, SN74LVTH543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS704C - AUGUST 1997 - REVISED APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

241	CATHEAS		ONDITIONS	SN	54LVTH	543	SN7	4LVTH	543	
PAI	RAMETER	IESI C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	٧
	XAM BUN	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0	.2		VCC-0.	2		
		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	WEN ALE	(SU 10 lb)	2.4	Turadori.	Pulled	V
VOH		V- 0.V	I _{OH} = -24 mA	2		rolled 8	0.8	D		V
		V _{CC} = 3 V	I _{OH} = -32 mA	WEST STREET	1.176	24,10 0	2	amil	cetail:	
	9.8	V 0.7.V	I _{OL} = 100 μA	d Okt bleki	9	0.2	2A		0.2	
		V _{CC} = 2.7 V	I _{OL} = 24 mA	Well strict	PAG	0.5	552		0.5	
V		67	I _{OL} = 16 mA	Tight step		0.4	O.A.		0.4	V
VOL		V OV	I _{OL} = 32 mA	Irel stat	1 20	0.5	212	800	0.5	V
		VCC = 3 V	I _{OL} = 48 mA	Deta migra		0.55	o-A			
		A.1. j	I _{OL} = 64 mA	自创 舒敬		12.	CONT.		0.55	
H. C.	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND		Š	±1			±1	
	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	nemine	24	10	MISSITES	OBTRI	10	
l _l			V _I = 5.5 V	N. C	7	20	70270711	O'BIAN E	20	μА
	A or B ports‡	V _{CC} = 3.6 V	VI = VCC		3	1			1	
THE	Ven = 2.7.V	V 0.6 = 3.5 V	V _I = 0	S V C	5 01	-5	HOR	9	-5	EASTAR .
loff		V _{CC} = 0,	V_I or $V_O = 0$ to 4.5 V	2	green and		(10.0	777	±100	μΑ
ha in	A or B ports	V _{CC} = 3 V	V _I = 0.8 V	75			75			μА
I(hold)	A of B ports	ACC = 2 A	V _I = 2 V	-75	A 10 8		-75	A .	H.	μА
lozpu		$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	0.5 to 3 V,		S to A	±100*	20		±100	μА
IOZPD	9:8 11 5:8 11	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = 1.5 \text{ V to o, V}_{O} = 1.5 V to $	= 0.5 to 3 V,			±100*			±100	μА
	0.2	8.8 r.1	Outputs high		100	0.19	30		0.19	qf .
Icc		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs low	9.		5			5	mA
		Al = ACC of GIAD	Outputs disabled	2.	of Man	0.19	34		0.19	
ΔICC§	8.6	V _{CC} = 3 V to 3.6 V, On Other inputs at V _{CC} or	e input at V _{CC} – 0.6 V, GND	S. I	8 to A	0.2	30		0.2	mA
Ci	0.8	V _I = 3 V or 0	69 178		4			4	-	pF
Cio		V _O = 3 V or 0	22 112	0.4	9	161813	30	9		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] Unused terminals at VCC or GND

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVTH543, SN74LVTH543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS704C - AUGUST 1997 - REVISED APRIL 1998

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	MYALVYMBAS	LVTHEAS 8	0.03529		SN54L	/TH543			SN74L	/TH543		9
					V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		3.3 V 3 V	V _{CC} = 2.7 V		UNIT
- 1			1 Ver-0.2	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	DRV
tw	Pulse duration,	LEAB or LEBA low	I se	3.3	Asp. A.	3.3		3.3	DOV.	3.3		ns
1		A or B before	Data high	0.4	Leve MQ_	0.4		0.4		0.4		Hox
	0-1	LEAB or LEBA↑	Data low	1	ure Est.	1.5		1	DOY .	1.5		ns
tsu	Setup time	A or B before	Data high	0.2	Augela	₹ 0.2		0.2		0.2		ns
		CEAB or CEBA↑	Data low	0.7	- A	1.2		0.7	VGC	1.2		
	FA:0	A or B after	Data high	1.5	3	0.6		1.5		0.6		
·V		LEAB or LEBA↑	Data low	1.3	0	1.5		1.3		1.5		304
th	Hold time	A or B after	Data high	1.6	Q"	0.5		1.6	00¥	0.5		ns
		CEAB or CEBA↑	Data low	1.4	Amad	1.6		1.4		1.6		

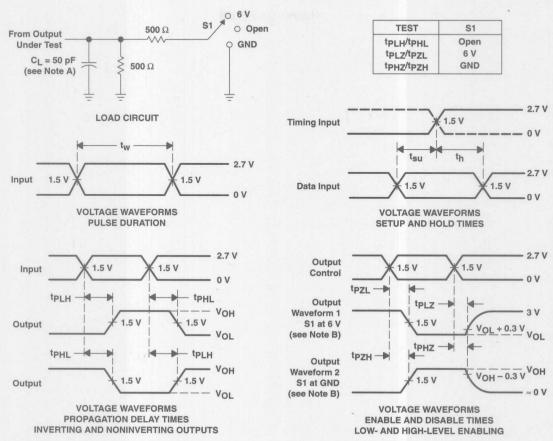
switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

				SN54L\	/TH543	4N		SN7	4LVTH	543	10 A	
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 ± 0.3 V		V	V _{CC} = 2.7 V		UNIT
Aq 0014			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	360
tPLH	A or B	B or A	1.2	3.9	T We	4.5	1.3	2.5	3.7	ahoq a	4.3	ns
tPHL	AOID	BOLA	1.2	3.9	37.0	4.5	1.3	2.5	3.7		4.3	115
tPLH	15	A or B	1.2	5.1	-	6.1	1.3	2.9	4.7		5.9	ns
tPHL	LE	AOIB	1.2	5.1	4	6.1	1.3	2.9	4.7		5.9	ns
t _{PZH}		A or B	1	5.1	W.	6.4	1.1	2.9	4.9		6.2	ns
tPZL	ŌĒ	AOFB	1	5.1	Q all atu	6.4	1.1	3.2	4.9		6.2	ns
tPHZ		A or B	1.9	5.6	wotan	6.2	2	3.4	5.3		5.9	ns
tPLZ	ŌĒ	AOFB	1.9	5.6	uta disali	6.2	2	3.7	5.3	E and a second	5.9	ns
tPZH		A or B	1.2	\$5.5	DOM IN	7	1.3	3.2	5.3		6.8	ns
tPZL	CE	AOFB	1.2	5.5		7	1.3	3.5	5.3		6.8	ns
tPHZ	CE	A an D	2.2	5.7		6.2	2.3	3.8	5.4		5.9	
tPLZ	CE	A or B	2.2	5.7		5.9	2.3	3.9	5.4		5.6	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION

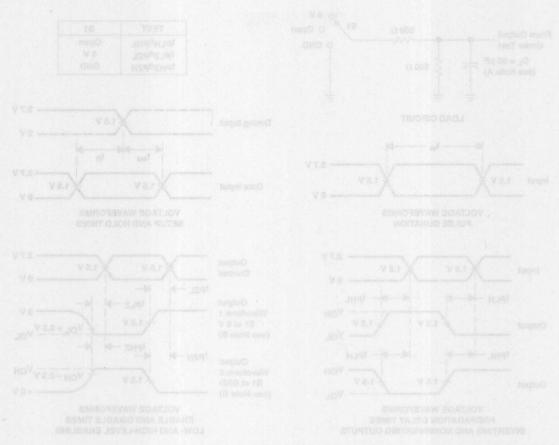


NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C. Includes proba and 30 paper and

S. Wirveldern 1 is for an outgat with internal occulings such that the output is low except when disabled by the output control.
Yorkstorm 2 is for an outgat with linear at conditions such that the output is high except when disabled by the output control.

All input paraes are supplied by generators travely the following chargos energy Presidents.

De The octuals are measured one at a une with one transition our my sourcement

Player 1, Load Choult and Vallage Waveforms

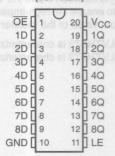


SN54LVTH573, SN74LVTH573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

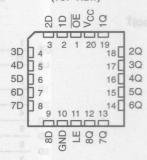
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH573...J OR W PACKAGE SN74LVTH573...DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTH573 . . . FK PACKAGE (TOP VIEW)



description

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the 'LVTH573 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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description (continued)

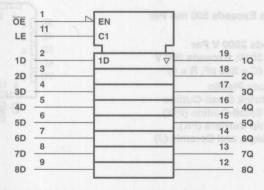
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH573 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

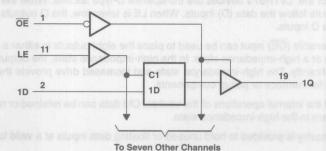
	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	X	Q ₀
Н	X	X	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH573, SN74LVTH573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, VO (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, Vo (see Note 1)	
Current into any output in the low state, Io: SN54LVTH573	96 mA
SN74LVTH573	
Current into any output in the high state, Io (see Note 2): SN54LVTH573	48 mA
SN74LVTH573	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Package thermal impedance, θ _{JA} (see Note 3): DB package	
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

Au 8			SN54LV	TH573	SN74LV	TH573	LINUT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	V-2 or V 2 0 = 0	2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2	20 = 110	2		٧
VIL	Low-level input voltage	V & of V & 0 = O	V Dat V b.)	0.8		0.8	V
VI	Input voltage		8 20 1 18	5.5	-	5.5	٧
ЮН	High-level output current	Tougus Non	.Val	-24		-32	mA
loL	Low-level output current	Walahahad	THE PARTY NAMED IN	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	A gig - DOA is India euch	200	YOU'V	200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54LVTH573, SN74LVTH573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS SCBS687D - MAY 1997 - REVISED APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TOLV		7507.0	CHRITICHIC	SNS	54LVTH	573	SN	74LVTH5	573	111117
PAI	RAMETER	TEST	CONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	-0.5	V _{CC} = 2.7 V,	I _I = -18 mA	(1	etoid	-1.2	/ state	tio-yea	-1.2	V
+ 0.5	-0.5 V to Voc	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0.	2	YES O	VCC-0.	.2	inge n	W.
m 88		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	IOW SI	and mi	2.4	yrus air	וווסדוו וו	V
VOH		V 0.V	I _{OH} = -24 mA	2						V
		VCC = 3 V	I _{OH} = -32 mA	S Or Base	E HIGHT	制版 1 0	2	ELITE COL	17 31 157 (1)	
11 7 10		V 07V	I _{OL} = 100 μA	1 Marie	11	0.2	. Litraria	mua ce	0.2	(79)
		V _{CC} = 2.7 V	I _{OL} = 24 mA		10 -	0.5	ineni	in none	0.5	
			I _{OL} = 16 mA	stol/Lea	al ar 0	0.4	samile	somedi	0.4	V
VOL		V 2V	I _{OL} = 32 mA			0.5			0.5	V
		VCC = 3 V	I _{OL} = 48 mA			0.55				
		average spinished	I _{OL} = 64 mA		· · · gla	Lagn	n ewis	nagms	0.55	12
a only, a	pritiés deorde éva	VCC = 0 or 3.6 V,	V _I = 5.5 V	spalles mun	nixem eli	10	ibra oan	eli delarti:	10	makinti
al leng	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	philos tedio	प्राप्त । ।	±1	DEMOYSD C	nit ito mul	±1	μА
l tomi	Data inputs	V _{CC} = 3.6 V	VI = VCC	one aboutes	area flows	1	n catio b	eve hiero	1	μА
	Data inputs	ata inputs VCC = 3.6 V	V _I = 0 pour state des	a the interior	giuo erl	-5	no swall	Mem 3	-5	
off		$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V	ni eathligh	10 El 600	stracmi	ormodil o	Parintaling	±100	μΑ
lea en	Data inputs	Vcc = 3 V	V _I = 0.8 V	75			75			μА
I(hold)	Data inputs	ACC = 2 A	V _I = 2 V	-75	A SPACE TO	Strain 4	-75	win se	PARTY PROPERTY	μА
lozh	SIND FOR THE STATE	V _{CC} = 3.6 V,	V _O = 3 V			5			5	μΑ
lozL	XAIA NIM	V _{CC} = 3.6 V,	V _O = 0.5 V			-5			-5	μΑ
lozpu	8.7 3.6	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	0.5 V to 3 V,			±100*	Pov kum	sliev ylig u level-n	±100	μА
lozpd	8.0	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = 1.5 \text{ V to o, V}_{O} = 1.5 V to $	0.5 V to 3 V,			±100*	ation Jug	ra lovní-s ientov li	±100	μА
Am	52 7 7	V _{CC} = 3.6 V,	Outputs high			0.19	era krotu	n keusterl	0.19	The same
lcc		$I_0 = 0$,	Outputs low			5	no dare	in leville	5	mA
Vien	O.F	V _I = V _{CC} or GND	Outputs disabled			0.19	ozin no	Germant for	0.19	DAIL
∆lcc‡			= 3 V to 3.6 V, One input at V _{CC} - 0.6 V, r inputs at V _{CC} or GND			0.2	n wit Gins	at guatev	0.2	mA
Ci		V _I = 3 V or 0			3			3	311	pF
Co		V _O = 3 V or 0	LOVA DOTO		7	Vision of	7 7 7 7 7	7		pF

^{*}On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH573, SN74LVTH573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS687D - MAY 1997 - REVISED APRIL 1998

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	te test	SN54L	VTH573	SN74L\		
		V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 2.7 V	UNIT
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t _W	Pulse duration, LE high	3	3	3	3	ns
t _{su}	Setup time, data before LE↓	0.7	0.6	0.7	0.6	ns
th	Hold time, data after LE↓	1.5	1.7	1.5	1.7	ns

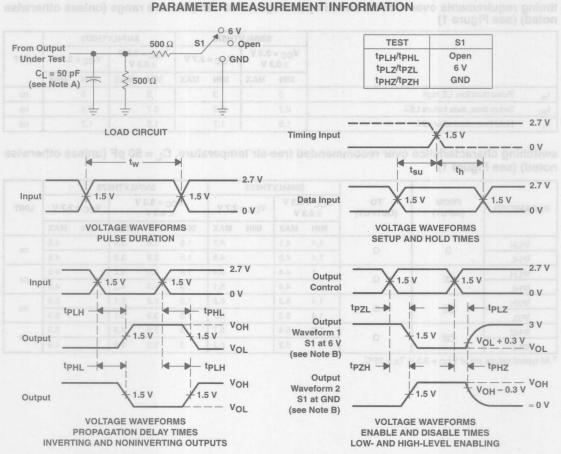
switching characteristics over recommended free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

Jersennie 2.7 V				SN54LV	/TH573			SN	74LVTH5	573	1.11			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.		V _{CC} =	2.7 V	V	CC = 3.3 ± 0.3 V	V	V _{CC} =	2.7 V	UNIT		
		SOATJOY	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX			
tPLH	D	Q	1.4	4.1		4.7	1.5	2.6	3.9		4.5	no		
tPHL	D	Q .	1.4	4.5		4.8	1.5	2.9	3.9		4.5	ns		
tPLH	N/E	Q	ustar1	4.4		5.4	1.9	2.9	4.2	1/-	4.9	no		
tPHL	V a.t LE	A	1.4	4.4		5.1	1.9	2.9	4.2	A	4.9	ns		
tPZH	ŌĒ	Q	1.4	5.2		6.2	1.5	3.2	5.1		5.9	no		
tPZL		OE	Q Iso	Q Iso	Q	1.4	5.2		6.2	1.5	3.9	5.1		5.9
tPHZ	ŌĒ	Q	1.2	5.4	S 19	5.7	2	3.5	4.9		5.5	ne		
tPLZ	OE	1	/ 0 m 18	5.2		5.2	2	3.2	4.6		4.9	ns		

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.







NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

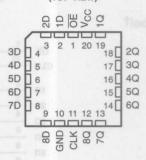
SCRS688C - MAY 1997 - REVISED MARCH 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH574...JOR W PACKAGE SN74LVTH574...DB, DW, OR PW PACKAGE (TOP VIEW)

OE [20	Vcc
1D [19	1Q
2D [3	18	2Q
3D [4	17	3Q
4D [16	4Q
5D [6	15	5Q
6D [7	14	6Q
7D [8	13	7Q
8D [9	12	8Q
GND [10	11	CLK
2.	-	THE RESERVE AND ADDRESS.	

SN54LVTH574...FK PACKAGE (TOP VIEW)



description

These octal flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVTH574 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.



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description (continued)

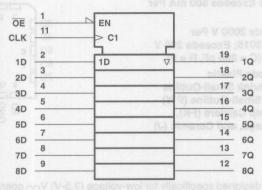
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH574 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH574 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each flip-flop)

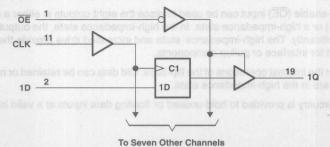
	INPUTS		OUTPUT
OE	CLK	D	Q
L	1	Н	Н
L	1	L	(Saur
L	HorL	X	Q ₀
Н	X	X	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, Vo (see Note 1)	
Current into any output in the low state, IO: SN54LVTH574	96 mA
SN74LVTH574	
Current into any output in the high state, Io (see Note 2): SN54LVTH574	48 mA
SN74LVTH574	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ _{JA} (see Note 3): DB package	
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T _{stq}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and VO > VCC.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV	TH574	SN74LVTH574		UNIT
			MIN	MAX	MIN	MAX	OINIT
Vcc	Supply voltage	V 6 or V 2 0 = 0 V	2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2	b = BO	2		٧
VIL	Low-level input voltage	VO = 0.5 V to 3 V.	Die Via.t	0.8		0.8	٧
VI	Input voltage		0 2 3 1 1 8	5.5		5.5	V
ЮН	High-level output current	rigin studioù	V.0.8	-24		-32	mA
loL	Low-level output current	Copula line	March	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	A 9:0 - 30a te trichi euro v	200	-00V	200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TALV	3.0		and the same of th	SNS	4LVTH5	74	SN	74LVTH5	74			
PAI	RAMETER	TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT		
VIK V B.O-		V _{CC} = 2.7 V,	I _I = -18 mA	(1	stold s	-1.2	/ .etate	10-101	-1.2	V		
-0.5 V to Voc + 0.5		V _{CC} = 2.7 V to 3.6 V,	to 3.6 V, I _{OH} = -100 μA			yris o	VCC-0.	2	llage r	W		
m 88		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	da woi	ent ni	2.4					
VOH		V 0V	I _{OH} = -24 mA	2		h k lu				V		
		VCC = 3 V	I _{OH} = -32 mA	7 31 -63389	at 13/6/11	DUTE THE	2	mu ean	i ji isirii			
-50 m		V 07V	I _{OL} = 100 μA		20	0.2			0.2	est.		
		V _{CC} = 2.7 V	I _{OL} = 24 mA		(G > v	0.5	towns	to many	0.5			
V/~.			I _{OL} = 16 mA	atoM ea	Blas B	0.4	pami le	rmarli	0.4	V		
VOL		V _{CC} = 3 V	I _{OL} = 32 mA			0.5	0.5			V		
		ACC = 2 A	I _{OL} = 48 mA			0.55						
			I _{OL} = 64 mA	pts i opre			n enune	18				
e prily, ar oner is n lj	miles aseria era	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	unites mun	bam elu	10	itans treb	if egod()	10			
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	alinet colle	(na 10-t	±1	edived p	tion of th	±1	μА		
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}	m engliss	NOU LISSUE	1	1			μ		
	Data inputs	VCC = 5.0 V	V ₁ = 0	s è ni st ju	s 0 rd at turgino ent men			Institute a	-5			
off		V _{CC} = 0,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5 \text{ V}$	ni pateluale	ip al aona	spodul.	umorti e	раскар	±100	μΑ		
I(hold)	Data inputs	V _{CC} = 3 V	V _I = 0.8 V	75				75				
'I(noia)	Data inputs	VCC = 0 V	V _I = 2 V	-75			-75			μА		
lozh	PARMANTALHES.	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V			5			5	μΑ		
lozL	XAM HIM	V _{CC} = 3.6 V,	V _O = 0.5 V			-5			-5	μĄ		
lozpu	2.7 1 7.2	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	0.5 V to 3 V,			±100*	age flov lugr	silov ylgs si leval-d	±100	μА		
lozpd		$\frac{\text{V}_{CC}}{\text{OE}} = 1.5 \text{ V to 0, V}_{O} =$	0.5 V to 3 V,			±100*	Mov ron	ni laval-e	±100	μΑ		
Am	5.6-	VCC = 3.6 V,	Outputs high			0.19	Hadrien Co.	e bambet	0.19	un's		
cc		I _O = 0,	Outputs low	5		5			mA			
(Aug.	Of.	V _I = V _{CC} or GND	Outputs disabled			0.19	Carle No.	Special to	0.19	Tukly.		
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One Other inputs at V _{CC} or 0				0.2	ato com	n quetan	0.2	mA		
Ci	100	V _I = 3 V or 0			3	SISTEM IN	91 119 119	3	40	pF		
Co	STATE OF THE OWNER, WHEN THE PARTY OF THE PA	V _O = 3 V or 0	Programmer of Charles	fer atti fattion	7	and and	S and stated to	7	San III and and a	pF		

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH574					SN74LVTH574			
			3.3 V 3 V	Vcc=	2.7 V	V _{CC} =	3.3 V 3 V	Vcc=	2.7 V	UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	1 5	
fclock	Clock frequency		150		150		150		150	MHz	
t _W	Pulse duration, CLK high or low	3.3		3.3		3.3	1	3.3		ns	
t _{su}	Setup time, data before CLK↑	2		2.4		2		2.4		ns	
th	Hold time, data after CLK↑	0.9		0.9		0.3	SHOW	0	1.014	ns	

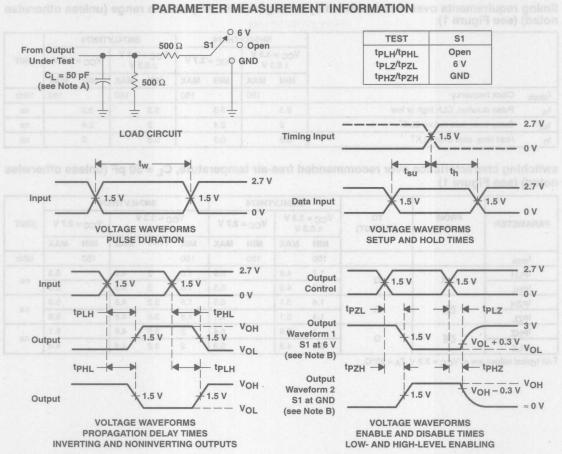
switching characteristics over recommended free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	X	作。八	lusinin	SN54LV	/TH574		LA.	SN7	74LVTH5	74	ASS	
	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V	± 0.3 V	V	V _{CC} = 2.7 V		UNIT
		CMA SUTSE	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
fmax			150		150		150			150		MHz
tPLH	CLK		1.7	4.9	V-4.5	5.9	1.8	3	4.5	James .	5.3	ns
^t PHL		V 8,1 Q	1.7	4.9		5.5	1.8	3	4.5		5.3	115
t _{PZH}		0	1.4	5.1		6.5	1.5	3.2	4.8		5.9	
tPZL	ŌĒ	Q 339	1.4	5.1		6.1	1.5	3.5	4.8	HIG	5.9	ns
tPHZ	ŌE VA	1	1	5.9	100.4	6.4	2	3.5	4.8		5.1	
tPLZ		Q	0.8	4.8	100	5.3	2	3.2	4.4		4.4	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{r} \leq 2.5$ ns, $t_{f} \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH646, SN74LVTH646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

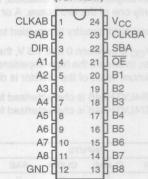
SCBS705C - AUGUST 1997 - REVISED APRIL 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Support Unregulated Battery Operation
 Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (JT) DIPs

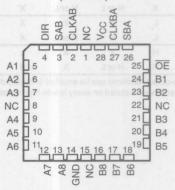
description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTH646 . . . JT OR W PACKAGE SN74LVTH646 . . . DB, DGV, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTH646 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The 'LVTH646 devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data can be stored in one register and/or B data can be stored in the other register.

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description (continued)

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH646 is characterized for operation from –40°C to 85°C.

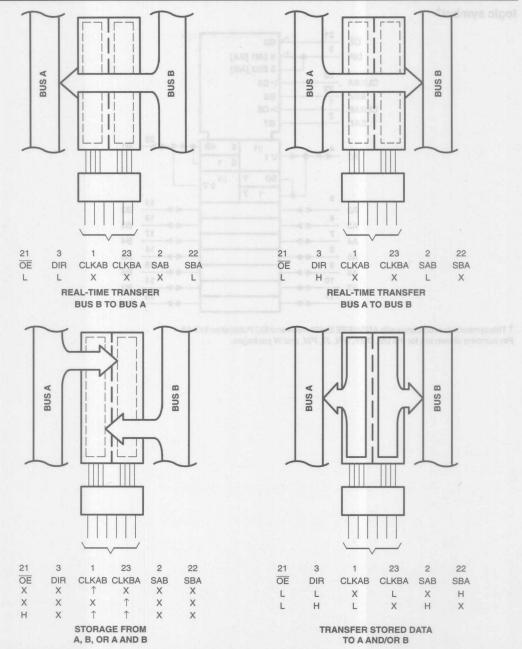
FUNCTION TABLE

		INP	UTS			DATA	A I/Os	OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OPERATION OR FUNCTION
X	X	1	X	X	X	Input	Unspecified [†]	Store A, B unspecified†
X	X	X	1	X	X	Unspecified [†]	Input	Store B, A unspecified†
Н	X	1	v ag	X	X	Input	Input	Store A and B data
Н	X	HorL	HorL	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	HorL	X	Н	Output	Input	Stored B data to A bus
L	Н	X	X	L	Х	Input	Output	Real-time A data to B bus
L	Н	HorL	X	H	X	Input	Output	Stored A data to B bus

[†] The data-output functions can be enabled or disabled by various signals at $\overline{\sf OE}$ and DIR. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.



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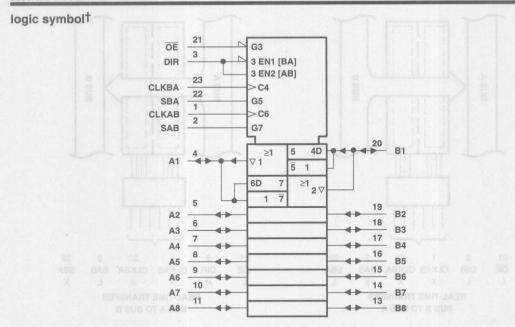


Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

Figure 1. Bus-Management Functions



SN54LVTH646, SN74LVTH646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS705C - AUGUST 1997 - REVISED APRIL 1998

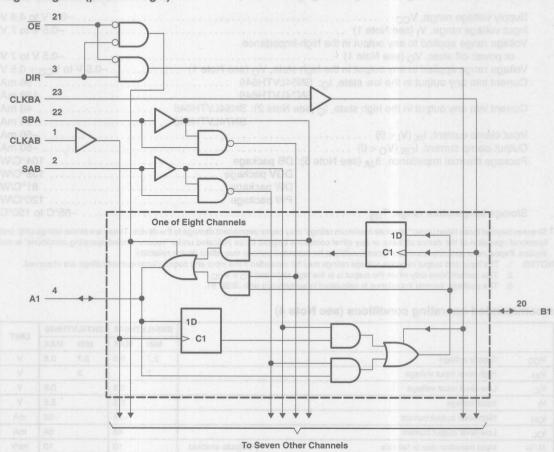


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.



SCBS705C - AUGUST 1997 - REVISED APRIL 1998

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}		-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 7 V
Voltage range applied to any output in the high-	impedance	
or power-off state, VO (see Note 1)		0.5 V to 7 V
Voltage range applied to any output in the high	state, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, Io: SN	54LVTH646	96 mA
SN	74LVTH646	128 mA
Current into any output in the high state, IO (see	e Note 2): SN54LVTH646	48 mA
		64 mA
Input clamp current, I _{IK} (V _I < 0)		
Output clamp current, IOK (VO < 0)		
Package thermal impedance, θ _{JA} (see Note 3):		
σ, ολ (DGV package	
	DW package	
	PW package	
Storage temperature range, T _{stq}		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$. 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV	TH646	SN74LV	TH646	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			. 0.8	had a	0.8	٧
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current	4 4 4 4		-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	JT, PNL and W poekages.	200	80 rd)	200	orie also	μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54LVTH646, SN74LVTH646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS705C - AUGUST 1997 - REVISED APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DASHTV	814546	ENDER VINERAL	SN	54LVTH	646	SN	74LVTH6	646	
PAI	RAMETER	V 6.5 = SOV	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	7 9 00	V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	٧
	NAM HIM I	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0	.2		VCC-0.	.2		
Milz		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4			2.4	yoneups	Makado.	V
VOH		8.8	IOH = -24 mA	2		wol to	told NUC	mation, 1	Pulse pa	V
		V _{CC} = 3 V	I _{OH} = -32 mA	rigiri ans	-1.2					
	2.2		I _{OL} = 100 μA	-Wol airs		0.2	e I BAN.	IC erose	0.2	
		V _{CC} = 2.7 V	I _{OL} = 24 mA		ABOLJO I	0.5	O neffe 8	10 A or 8	0.5	
			I _{OL} = 16 mA			0.4			0.4	.,
VOL		eair temperature	I _{OL} = 32 mA	remmen	0097	0.5	ollah	araclo	0.5	V
		VCC = 3 V	I _{OL} = 48 mA	(2 8	nugn	0.55	Deron	881/8	PERK!	
		KTVJANIR J	I _{OL} = 64 mA						0.55	
Taxu	0.44	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Vol.	01	±1	MO	199	±1	no Ares
	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V		QUE	10	(IU	((4))	10	
l _l	KAM RIM	KASI PYYT HUN	V _I = 5.5 V	P M		20			20	μΑ
	A or B ports‡	V _{CC} = 3.6 V	V _I = V _{CC}	0 N - F		1			13	
	0.6	1.8 2.1 4.1	V _I = 0		200	-5	10 AB	5/10	-5	
loff	8.8	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V				EAV	LU	±100	μΑ
. 00	A - D	V 0 V	V _I = 0.8 V	75	S an		75		L. I	197
I(hold)	A or B ports	VCC = 3 V	V _I = 2 V	-75			-75			μΑ
lozpu	8	V _{CC} = 0 to 1.5 V, V _O = OE = don't care	0.5 V to 3 V,	87	-8 to-	±100*	4UAR)	SBA	±100	μА
lozpd	8.6 8.5	V _{CC} = 1.5 V to 0, V _O = OE = don't care	0.5 V to 3 V,		8.10	±100*	- 49	5	±100	μА
	1.8	1 23 69 57	Outputs high	ST.		0.19			0.19	unif
lcc		$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low	90	210	5	3	9	5	m/
	0.8	VI = VCC OF GIVE	Outputs disabled	s F		0.19			0.19	
∆I _{CC} §	8.8	V _{CC} = 3 V to 3.6 V, One Other inputs at V _{CC} or		St	No 10	0.2		u ·	0.2	m/
Ci	0.0	V _I = 3 V or 0			4	KEE	A	4	-	pF
Cio	land the same of t	V _O = 3 V or 0			9			9		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ Unused terminals at V_{CC} or GND

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

Tiral	SNT4LYTH646				SN54LV	TH646	0.7523		SN74LVTH646			
				V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		2.4		150	Hot	150	VYS:	150		150	MHz
t _W	Pulse duration, CLK high	or low	8	3.3	1-24 m	3.3		3.3		3.3		ns
	Setup time,	THE STATE	Data high	1.3	m \$6-=	1.6		1.2	-00x	1.5		
tsu	A or B before CLKABT or	· CLKBA1	Data low	1.9	Au 001	2.6		1.6		2.2		ns
th	Hold time, A or B after CL	KAB↑ or C	LKBA [↑]	1.2	Amas a	1.2		0.8	1004	0.8	18	ns

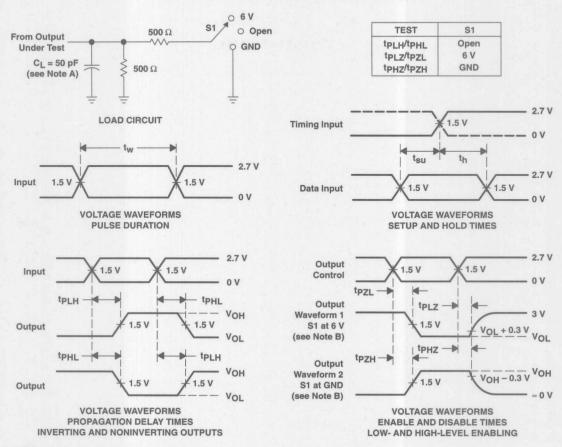
switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 2)

				SN54L\	/TH646	TOL		SN7	4LVTH6	346	UNIT						
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V								Vcc=	2.7 V	V _{CC} = 3.3 V ± 0.3 V		V	V _{CC} = 2.7 V	UNIT
		65	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN MAX	1						
fmax			150		150	e IV	150	Vac:	erev!	150	MH						
tPLH	CLKBA or	A or B	1	5	0	5.9	1.8	3.1	4.7	5.6	ns						
tPHL	CLKAB	AOIB	1.5	5	0=pV	5.9	1.8	3.1	4.7	5.6	IIS						
t _{PLH}	A or B	B or A	1.1	4.9	V a.o	5.6	1.3	2.3	3.5	4.1							
tPHL	AOIB	BOLA	1.2	4.8	VS	5	1.3	2.4	3.5	4.1	ns						
t _{PLH}	ans asst	A or B	1.1	5.3	Ne.	6.3	1.5	3	4.9	6							
tPHL	SBA or SAB‡	AOIB	1.3	5.3		6.3	1.5	3.3	4.9	6	ns						
^t PZH		A or B	1	5.4	-V 6)	6.7	01.1	3.1	5.2	6.5	ns						
tPZL	ŌĒ	AOIB	1	5.6		6.7	1.1	3.4	5.2	6.5	TIS						
tPHZ		A or B	1.7	6	right stu	6.5	2.3	3.9	5.5	6.1							
tPLZ	OE	AOLP	2.2	6.3	Wel 8)0	6.5	2.3	4	5.5	5.9	ns						
tPZH	DIR	A or B	1.2	5.6	BEID BILL	6.8	1.3	3.4	5.2	6.6	ns						
tPZL	DIR	AOIB	1.2	5.7	- pay t	6.8	1.3	3.6	5.2	6.6	ns						
tPHZ	DIR	A or B	1.1	5.8		6.9	1.5	3.2	5.6	6.7	no						
tPLZ	DIN	AOLP	1.4	6.1		6.6	1.5	3.8	5.6	6.3	ns						

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

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PARAMETER MEASUREMENT INFORMATION

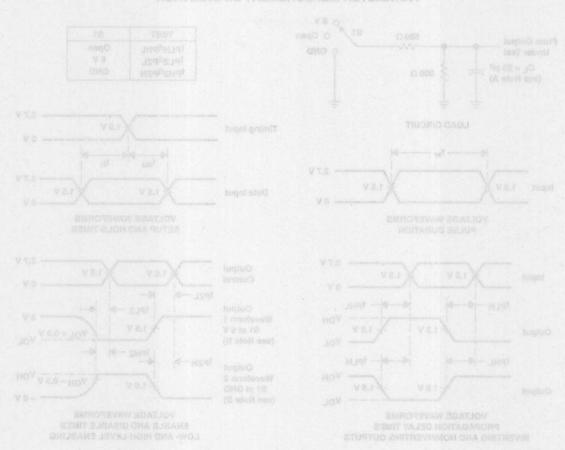


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C. Indudes probe and jig edoactance

Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

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Floure 2, Load Circuit and Voltage Wavelonns



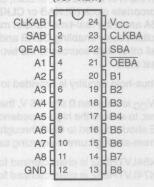
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V
 Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (JT) DIPs

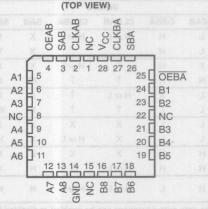
description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTH652 . . . JT OR W PACKAGE SN74LVTH652 . . . DB, DGV, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTH652 . . . FK PACKAGE



NC - No internal connection

The 'LVTH652 devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input selects real-time data and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH652 devices.

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description (continued)

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input; therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54LVTH652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH652 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

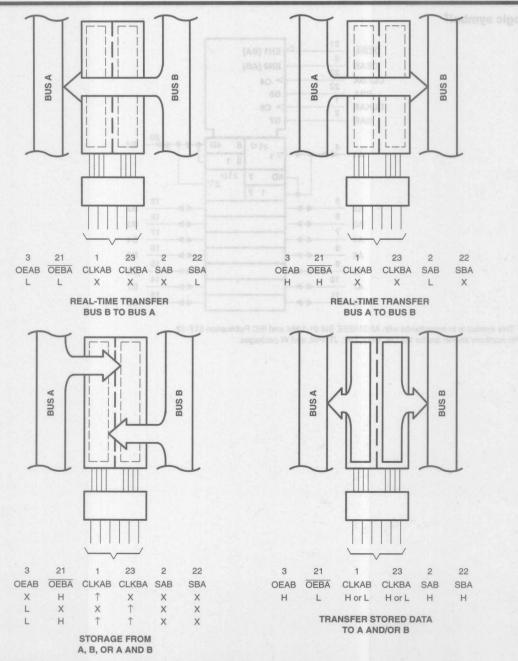
		INPU'	TS			DAT	TA I/OT	OPERATION OF FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OPERATION OR FUNCTION
L	Н	HorL	HorL	X	X	Input	Input	Isolation
L	Н	10 1	Z CA DIS	X	X	Input	Input	Store A and B data
X	Н	88 To 88	HorL	X	X	Input	Unspecified [‡]	Store A, hold B
Н	H	1	1	X‡	X	Input	Output	Store A in both registers
L	X	HorL	1	X	X	Unspecified [‡]	Input	Hold A, store B
L	L H	1	1	X	X‡	Output	Input	Store B in both registers
L	o L fi	X	X	X	L	Output	Input	Real-time B data to A bus
L	. L	X	HorL	X	Н	Output	Input	Stored B data to A bus
Н	Н	X	X	m4 a	X	Input	Output	Real-time A data to B bus
Н	Н	HorL	X	Н	X	Input	Output	Stored A data to B bus
Н	L	H or L	HorL	Н	Н	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

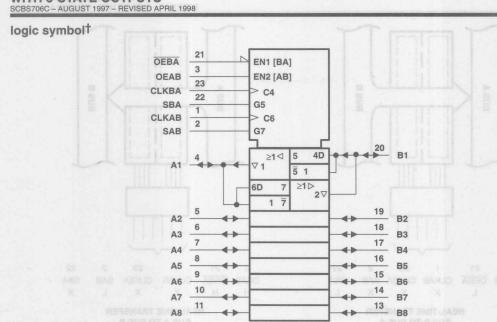
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Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

Figure 1. Bus-Management Functions



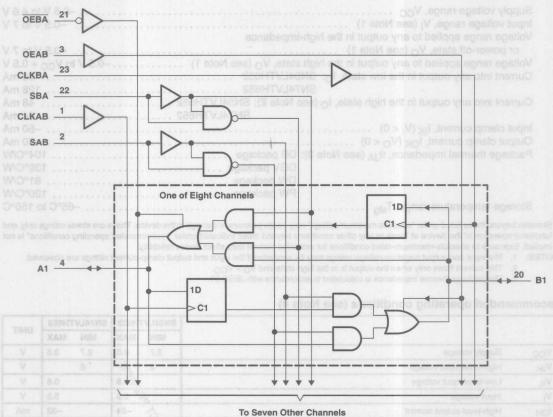


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.



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logic diagram (positive logic) and emissioned his east palls sego tevo sonder municipal studies of



Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		
Input voltage range, V _I (see Note 1) Voltage range applied to any output in the high-		–0.5 V to 7 V
or power-off state, VO (see Note 1)		0.5 V to 7 V
Voltage range applied to any output in the high		
Current into any output in the low state, Io: SN	54LVTH652	96 mA
		128 mA
Current into any output in the high state, IO (see	e Note 2): SN54LVTH652	48 mA
	SN74LVTH652	64 mA
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Output clamp current, IOK (VO < 0)		
Package thermal impedance, θ _{JA} (see Note 3):	DB package	104°C/W
	DGV package	139°C/W
ger men stelle stelle stelle stelle stelle sider men stelle stelle desse dette stelle stelle stelle stelle stelle	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stq}		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		harmon and	SN54LV	TH652	SN74LV	TH652	LINUT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	12	2		٧
VIL	Low-level input voltage			\$0.8		0.8	٧
VI	Input voltage		1	5.5		5.5	٧
ГОН	High-level output current	98 of	1	-24		-32	mA
IOL	Low-level output current	ione W paci	120,000	48	in are for	64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	00	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate		200	1911	200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

-	\$80117	SN74LV	STENSE STEEL	SNS	4LVTH	552	SN	74LVTH6	552	UNIT
PAF	RAMETER	VEE SOOV TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2		SN74LVTH652 MIN TYPT MAX -1.2 /CC-0.2 2.4 2 0.2 0.5 0.4 0.5 0.5 41 10 20 1 -5 ±100 75 -75 ±100 0.19 5 0.19 0.2	-1.2	V
	XAW NIE	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0.	2		VCC-0	.2		
SHIA.		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4			2.4	variation of	17.26004.0	V
VOH		V 0V	I _{OH} = -24 mA	2	-	W-01-10	TOUT HUST	house	D SEIDSI	V
		VCC = 3 V	I _{OH} = -32 mA	odiu entr			2	,801	Setup ti	
	100000000000000000000000000000000000000	V 07V	I _{OL} = 100 μA	VACH BUIDS		0.2	O TENTO	ALC BRIDING	0.2	
		V _{CC} = 2.7 V	I _{OL} = 24 mA	17	enuun	0.5	C) 16/16 8	3 10 A 31	0.5	
V			I _{OL} = 16 mA			0.4			0.4	V
VOL		attricted the	I _{OL} = 32 mA	Disertant	0091	0.5	Oliselle	27.75.16	0.5	V
		VCC = 3 V	I _{OL} = 48 mA	100.00	ARITH A	0.55	West Offi	SCHOOL VA	No.	
		SHTALVTHO	I _{OL} = 64 mA			12			0.55	
THUL	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Ves.	S	±1	MO	84	±1	MARKS
	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	-	20	10	0.00	1911)	10	
lį	AAR WE	SAME THE MEN	V _I = 5.5 V	2,000	1	20			20	μА
	A or B ports‡	V _{CC} = 3.6 V	V _I = V _{CC}		3	1			1	
an	8.0	1,8 1,6 8,1	V _I = 0	0	8 10	-5	10 AE	DERO.	-5	PE
loff	1 8.0	V _{CC} = 0,	V_{1} or $V_{0} = 0$ to 4.5 V	Q			GAU		±100	μА
lia in	A or B ports	V _{CC} = 3 V	V _I = 0.8 V	75	A.10	8	75	×A.	1	μА
II(hold)	A of B ports	ACC = 2 A	V _I = 2 V	-75			-75			μΑ
lozpu		$V_{CC} = 0$ to 1.5 V, $V_O = OE/OE = don't care$	0.5 to 3 V,			±100*	\$BAB 1		±100	μА
IOZPD	8.8	$V_{CC} = 1.5 \text{ V to 0, V}_{O} = OE/OE = don't care}$	0.5 to 3 V,	1-1	A	±100*	ASI	10	±100	μА
	11.8	2.3 3.6 5.5	Outputs high	88		0.19			0.19	(ref)
Icc		$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low	22		5	Pict	10	5	mA
		AI = ACC OL CIAD	Outputs disabled	SHIP		0.19	Fig. 10		0.19	
Δlcc§	7.6 7.8	V _{CC} = 3 V to 3.6 V, One Other inputs at V _{CC} or		91		0.2	San.		0.2	mA
Ci	5.8	V _I = 3 V or 0	180		4		MA	4		pF
Cio		V _O = 3 V or 0	A CONTRACTOR OF THE REAL PROPERTY.	1	9		001	9	Savina 1	pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_{A} = 25°C. ‡ Unused terminals at V_{CC} or GND

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS706C - AUGUST 1997 - REVISED APRIL 1998

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

	THE62 SMY41,VTH682			SN54L\	/TH652			888			
			V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	V _{CC} =	V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	- 20
fclock	Clock frequency	3.2		150	= uni	150	MINI	150		150	MHz
t _W	Pulse duration, CLK high or low	1 9	3.3	Ani 102-	3.3		3.3		3.3		ns
	Setup time,	Data high	1.3	A-1.0	1.6		1.2	* OOV	1.5		
tsu	A or B before CLKAB1 or CLKBA1	Data low	1.9	8/6/	2.6		1.6		2.2		ns
th	Hold time, A or B after CLKAB↑ or CL	KBA↑	1.2	D.m. 50	1.2		0.8	- COV	0.8		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

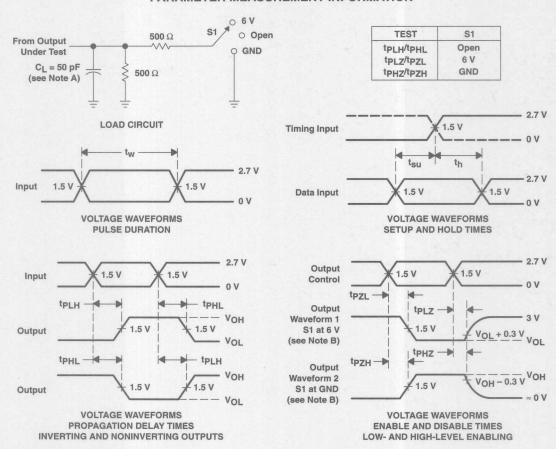
MHz	52	4LVTH6	SN7		= 1001	TH652	SN54LV				0.85				
	V _{CC} = 2.7 V	V ggV	V _{CC} = 3.3 V ± 0.3 V		2.7 V	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V						TO (OUTPUT)	FROM (INPUT)	PARAMETER
	MIN MAX	MAX	TYPT	MIN	MAX	MIN	MAX	MIN	100		Nu 08				
	150		Mar	150	Jan W.	150		150			fmax				
200	5.6	4.7	3.1	1.8	5.9		5	1.7	A or B	CLKBA or	tPLH				
ns	5.6	4.7	3.1	1.8	5.9	March W	5	1.7	AOFB	CLKAB	tPHL				
ns	4.1	3.5	2.3	1.3	4.3	V.A.	3.7	1.2	B or A	A or B	tPLH				
	4.1	3.5	2.4	1.3	4.3		3.7	1.2	BOLA	AOFB	tPHL				
	6	4.9	3.1	1.5	6.3	15	5.2	1.4	A or B	one ornt	t _{PLH}				
ns	6	4.9	3.4	1.5	6.3	Q2"	5.2	1.4	A OF B	SBA or SAB‡	tPHL				
no	6.5	5.2	2.9	1,1_0	6.7		5.4	1	core A	OED.	[†] PZH				
ns	6.5	5.2	3.1	1.1	6.7	1	5,4	1	OUT A	OEBA	t _{PZL}				
ns	6.1	5.5	3.5	2.3	6.5	rigiri ah	5.9	2.2	71.0 A	OED4	tPHZ				
115	5.9	5.5	3.7	2.3	6.3	vyol eh	5.9	2.2	^	OEBA	tPLZ				
ns	5.7	4.7	3	1.3	5.9	ida sib an	4.9	1.2	В В	OEAB	tPZH				
115	5.7	4.7	3.3	1.3	5.9	Voc-0	4.9	1.2	В	OEAB	tPZL				
ns	6.7	5.6	3.6	1.5	7		5.8	1.4	P	OEAB	tPHZ				
118	6.3	5.6	3.7	1.5	6.6		5.9	1.4	В	OEAD	tPLZ				

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] These parameters are measured with the internal output state of the storage register opposite that of the bus input.

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PARAMETER MEASUREMENT INFORMATION

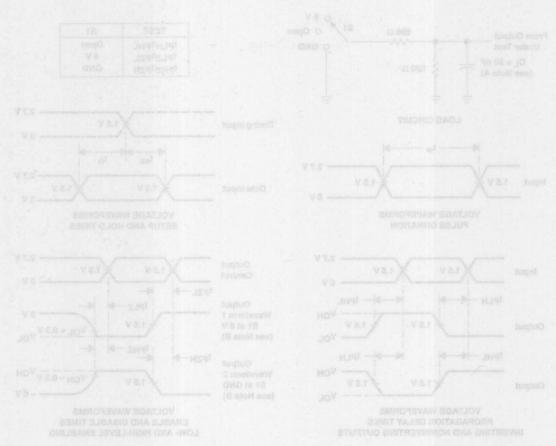


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Or includes probe and its capacitance.
- Waveform 1 is for an output with internal conditions such that the output to be secapt when disabled by the output control.

 Waveform 2 is for an output with the man conditions such that output is both secapt when disabled by the output control.
- Vavolorm 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

 All input pulses are supplied by generators having the following characteristics: PRR a 10 MHz. Zo = 50 Ω, to ≤ 2.5 ns., to ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.

Flaure 2. Load Circuit and Voltage Waveforms



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State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V **Operation and Low Static Power** Dissipation

- High-Impedance State During Power Up and Power Down
- Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- **Support Unregulated Battery Operation** Down to 2.7 V
- **Power Off Disables Outputs, Permitting** Live Insertion
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages. Ceramic Chip Carriers (FK), and Ceramic (JT) DIPs

description

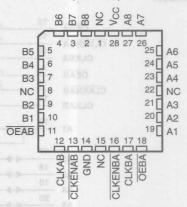
These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

UNLESS OTHERWISE NOTED this document contains PRODUCTION

SN54LVTH2952 . . . JT PACKAGE SN74LVTH2952 . . . DB. DGV. DW. OR PW PACKAGE (TOP VIEW)



SN54LVTH2952 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The 'LVTH2952 devices consist of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input, provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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description (continued)

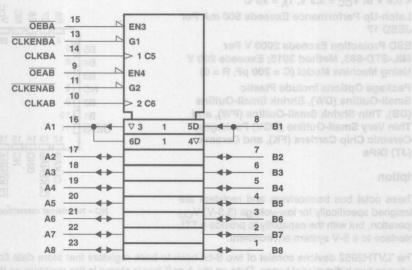
The SN54LVTH2952 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH2952 is characterized for operation from –40°C to 85°C.

FUNCTION TABLET

	INPUT	S		OUTPUT
CLKENAB	CLKAB	OEAB	A	В
Н	X	L	X	B ₀ ‡
X	HorL	L	X	B ₀ ‡
L	1	L	L	L
SAL .	1	L	Н	Н
X	X	Н	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA. CLKBA. and OEBA.

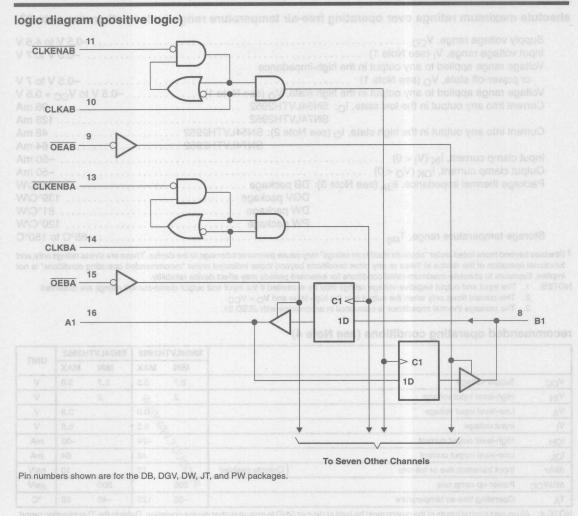
logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DGV, DW, JT, and PW packages.

[‡] Level of B before the indicated steady-state input conditions were established

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}		
Input voltage range, V _I (see Note 1)		
Voltage range applied to any output in the high-		
or power-off state, VO (see Note 1)		0.5 V to 7 V
Voltage range applied to any output in the high	state, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, Io: SN	154LVTH2952	96 mA
	174LVTH2952	
Current into any output in the high state, IO (se	e Note 2): SN54LVTH2952	48 mA
	SN74LVTH2952	64 mA
Input clamp current, I _{IK} (V _I < 0)		
Output clamp current, IOK (VO < 0)		
Package thermal impedance, θ _{JA} (see Note 3):		
	DGV package	
	DW package	
	PW package	
Storage temperature range, T _{sto}		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVT	H2952	SN74LVT	H2952	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	42	2		٧
VIL	Low-level input voltage			6.8		0.8	٧
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current		L A	-24		-32	mA
loL	Low-level output current		3	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	,0'	_10	March ages on	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		2 200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	CERCIATA	INTERES - SINTERES	OND TO VIO	SN5	4LVTH2	952	SN7	4LVTH2	952	
PA	RAMETER	V 8.6 # SOV	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	V
	NAM HIM	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0	.2		VCC-0	.2		
st the		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4			2.4	yaneups	Classic b	V
VOH		8.8	I _{OH} = -24 mA	2	21			and the state of	San Contractor	V
		V _{CC} = 3 V	I _{OH} = -32 mA	wet 24.8			2			
	18	V 07V	I _{OL} = 100 μA	rigari siles		0.2	4.5		0.2	
		V _{CC} = 2.7 V	I _{OL} = 24 mA	wor also		0.5			0.5	
		2.7	I _{OL} = 16 mA	don't sam		0.4	And little		0.4	V
VOL		V 2V	I _{OL} = 32 mA	wal sin		0.5		1.8	0.5	V
		V _{CC} = 3 V	I _{OL} = 48 mA			0.55	A OF 18 A			
			I _{OL} = 64 mA			CUL	refly 30	Maria	0.55	
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1			±1	
	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	SHEETING THE	0000	10	oliahic	rio erie	10	
lį.			V _I = 5.5 V	17.0		20	Deader	earry	20	μА
	A or B ports‡	V _{CC} = 3.6 V	VI = VCC		2	1			1	
	1	V 6.0 = 00 V	V _I = 0	SV S	0.7	-5	100	88	-5	
loff		$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5 V	Q"	Tanalli	10)	(11)	WH)	±100	μΑ
fra . r.s	A or B ports	V _{CC} = 3 V	V _I = 0.8 V	75			75			μА
I(hold)	A OI B poils	VCC = 3 V	V _I = 2 V	-75			-75			μΑ
lozpu	5.3	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	= 0.5 V to 3 V,	91	(8 no /	±100*	10 A8		±100	μΑ
IOZPD	5.8	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = 1.5 V to $	= 0.5 V to 3 V,	T T	8107	±100*	aAjāō n	ARBO	±100	μА
	6.9	1,3 8.8 6,4	Outputs high	SELE		0.19			0.19	lest.
Icc		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs low	e l'I	H 10 /	5	SIMPSIU III	NAME OF THE OWNER, OWNE	5	mA
		VI - VCC or GIVE	Outputs disabled			0.19	= 25 C	This ons	0.19	
ΔICC§		V _{CC} = 3 V to 3.6 V, Or Other inputs at V _{CC} or	ne input at V _{CC} – 0.6 V, GND			0.2			0.2	mA
Ci		V _I = 3 V or 0			4			4		pF
Cio		V _O = 3 V or 0			9	1- 11		9		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at VCC = 3.3 V, TA = 25°C.

[‡] Unused terminals at V_{CC} or GND

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirement over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

THELL				SN54LVTH2952				SN74LV	TH2952	· ·	49		
					V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		3.3 V 3 V	V _{CC} = 2.7 V		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequen	icy	Ag II		150	= lard	150	NTS=	150		150	MHz	
	D. I		CLK high	3.3	Am AS-	333		3.3		3.3		HO	
t _W	Pulse duration		CLK low	3.3	Am Sev	3.3		3.3	DOAL	3.3		ns	
	150	1. 18.0	Data high	1.6	Autor	2.2		1.5		2.1			
	20	A or B before CLK↑	Data low	1.6	An A	2.2	2.2 1.5	2.1					
tsu	Setup time CE befor	==	Data high	1.6	A A	1.9		1.5		1.8		ns	
		CE before CLK↑	Data low	2	0	2.6		1.9		2.5		10,	
	Lia lai Alassa	A or B after CLK↑		1	Am D)	0.2		1	201	0.2			
th	Hold time	Hold time CE after CLK↑		1.2	Am as	0.2		1.2		0.2		ns	

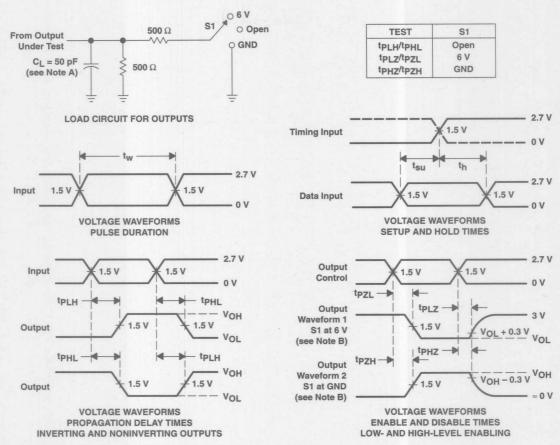
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

			SN54LVTH2952				SN74LVTH2952						
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V	V _{CC} = 2.7 V		UNIT	
	75		MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
fmax	-75		150		150	S=(V)	150		JU!	150	100	MHz	
tPLH	CLKBA or CLKAB	CLKBA or	A or B	1.2	4.8	.S' a	5.5	1.3	2.9	4.6		5.3	no
t _{PHL}		AOIB	1.2	4.8	24	5.5	1.3	3.1	4.6	L.B.	5.3	ns	
tPZH	OFDA OFAD	A or B	1	4.8	N. S.	5.9	0\1.1	2.6	4.6		5.8		
tPZL	OEBA or OEAB	AOIB	1	4.8		5.9	1.1	3	4.6		5.8	ns	
tPHZ	OEBA or OEAB	A or B	1.2	5.6	rigid at	6	1.3	3.6	5.4		5.9		
tPLZ		AOFB	1.5	2 5.4	wetal	5.6	1.6	3.6	5.1		5.3	ns	

† All typical values are at T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION



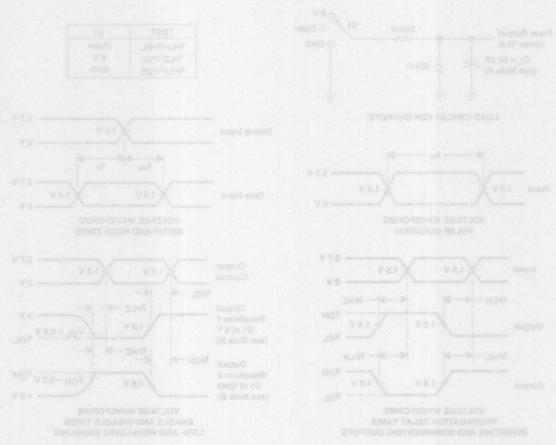
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , t_{f} \leq 2.5 ns, t_{f} \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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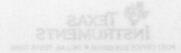
PARAMETER MEASUREMENT IMPORMATION



NOTES: A. O. Includes probe and its ospecitanos

- Naveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- sulers shireu qizis hiimtida = 02 izuwi ni isiniziri tone tersebeb Buluvayer adi Bulua sosaranab ka pendone wa sasindizidin kw
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1, Load Circuit and Voltage Wayerorms



etriateo0

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	3.3-V ABT 16-Bit Bus Transceivers With 3-State Outputs SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-Bit Transgerent D-Type Latches With 3-State Output: SN54LVTH162373, SN74LVTH162373	
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The SN74LVTH 6500, SN54LVTH16501, SN74LVTH18501, and SN74LVTH16535 are shown as product proview in this data book. The corresponding production data LVT data sheets for these devices are available through the Ti frome pape at fatter/lywww.ft.com/.

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[†] The SN74LVTH16500, SN54LVTH16501, SN74LVTH16501, and SN74LVTH16835 are shown as product preview in this data book. The corresponding production data LVT data sheets for these devices are available through the TI home page at http://www.ti.com/.

SN54LVTH16240, SN74LVTH16240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS684B - MARCH 1997 - REVISED MARCH 1998

•	Members of the Texas Instruments Widebus™ Family	SN54LVTH16240 WD PACKAGE SN74LVTH16240 DGG OR DL PACKAGE
nyo	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation	(TOP VIEW) 10E
0.	(E. W. Innest and Output Valtages With	GND [4 45] GND 1Y3 [5 44] 1A3 1Y4 [6 43] 1A4
•	Support Unregulated Battery Operation Down to 2.7 V	V _{CC} 7 42 V _{CC} 2Y1 8 41 2A1
•	and Power Down	2Y2 9 40 2A2 GND 10 39 GND
•	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C	2Y3 11 38 2A3 2Y4 12 37 2A4 3Y1 13 36 3A1
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors	3Y2 14 35 3A2 GND 15 34 GND
•	Power Off Disables Outputs, Permitting Live Insertion	3Y3 16 33 3A3 3Y4 17 32 3A4 V _{CC} 18 31 V _{CC}
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise	4Y1 19 30 4A1 4Y2 20 29 4A2
•	Flow-Through Architecture Optimizes PCB	GND 21 28 GND 4Y3 22 27 4A3
•	Latch-Up Performance Exceeds 500 mA Per JESD 17	4Y4 23 26 4A4 4OE 24 25 3OE
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)	
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings	

description

These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH16240 devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The devices provide inverting outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

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SN54LVTH16240, SN74LVTH16240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

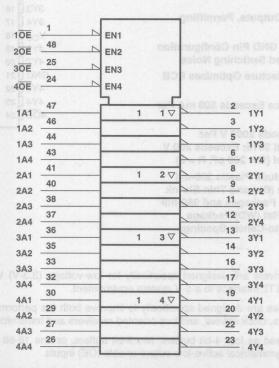
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH16240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INP	UTS	OUTPUT
OE	Α	Y
L	Н	L inc
L	L	Н
Н	X	Z

logic symbol†

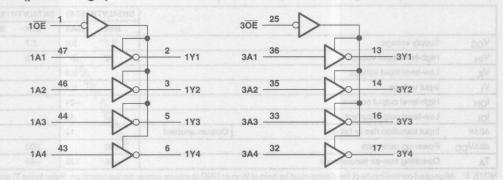


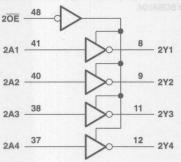
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

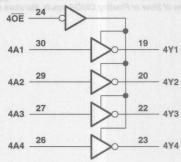


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logic diagram (positive logic)







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high-impedance
or power-off state, V _O (see Note 1)
Voltage range applied to any output in the high state, V _O (see Note 1)0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, Io: SN54LVTH16240
SN74LVTH16240
Current into any output in the high state, I _O (see Note 2): SN54LVTH16240
SN74LVTH16240
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0)
Package thermal impedance, θ _{JA} (see Note 3): DGG package
DL package 94°C/W
Storage temperature range, Teta

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



SN54LVTH16240, SN74LVTH16240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

				SN54LVTI	H16240	SN74LVTH16240		LIMIT
	P 300		MIN	MAX	MIN	MAX	UNIT	
Vcc	Supply voltage			2.7	3.6	2.7	3.6	V
VIH	High-level input voltage	- TAE	141	2	12.	2		V
VIL	Low-level input voltage				8.0		0.8	V
VI	Input voltage	SAZ -SP	571	-bc -	5.5	- sar	5.5	V
ЮН	High-level output current			1	-24		-32	mA
loL	Low-level output current	38	5 193	3	48	- FAY	64	mA
Δt/Δν	Input transition rise or fall rate		Outputs enabled	0	10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	22	3	200		200		μs/V
TA	Operating free-air temperature			-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Supply voltage range, V_{CC}

Supply voltage range, V_{CC}

Output voltage range applied to any output in the high state, V_C (see Note 1)

Voltage range applied to any output in the high state, V_C (see Note 1)

Voltage range applied to any output in the high state, V_C (see Note 1)

Current into any output in the high state, I_C (see Note 1)

Current into any output in the high state, I_C (see Note 2): SNS4LVTH16240

Current into any output in the high state, I_C (see Note 2): SNS4LVTH16240

Current into any output in the high state, I_C (see Note 2): SNS4LVTH16240

SN74LVTH16240

Gamber into any output in the high state, I_C (see Note 2): SNS4LVTH16240

SN74LVTH16240

SN74LVTH16240

Gamber into any output in the high state, I_C (see Note 2): SNS4LVTH16240

SN74LVTH16240

SN74LVTH16240

Gamber into any output in the high state, I_C (see Note 2): SNS4LVTH16240

SN74LVTH16240

SN74LVTH16240

Gamber into any output in the high state, I_C (see Note 3): DGG package themset increase increase in the see of any other conditions beyond those lights in the endowed the service of the

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH	116240	SN74LVTH	LIMIT			
		TEST CON	MIN TYP	† MAX	MIN TYPT	MAX	UNIT			
		V _{CC} = 2.7 V,	I _I = -18 mA	(13/4	-1.2	(TURIN)	-1.2	٧		
	-XAM MIM	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.2		V _{CC} -0.2				
Vон		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	,	2.4	1 6	rol .		
		27.9	I _{OH} = -24 mA	2			1 1	V		
		VCC = 3 V	I _{OH} = -32 mA		a la la	2	1 19	Edj -		
Vol	4.8		I _{OL} = 100 μA	T. I	0.2		0.2	Set		
		V _{CC} = 2.7 V	I _{OL} = 24 mA	0.5		1976	0.5			
		3 2 32 42	I _{OL} = 16 mA		0.4		0.4	191		
		0.5	I _{OL} = 32 mA		0.5		0.5	V		
		V _{CC} = 3 V	I _{OL} = 48 mA	0.55		values are at Vog = 3.3		soloy!		
			I _{OL} = 64 mA	NACINA DERICH	d ourra eu	two outputs out				
lμ		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V		<u>\$</u> 10		10			
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND		,5 ±1		±1			
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}		2 1		μΑ			
			V _I = 0	A	- 5		-5			
loff		V _{CC} = 0, V _I or V _O = 0 to 4.5 V		3			μА			
In	Data inputs	V _{CC} = 3 V	V _I = 0.8 V	75,0		75				
I(hold) Data inputs		ACC = 2 A	V _I = 2 V	-75		-75	μΑ			
lozh		V _{CC} = 3.6 V,	V _O = 3 V		5		μА			
lozL		V _{CC} = 3.6 V,	$= 3.6 \text{ V}, \qquad \qquad \text{V}_{\text{O}} = 0.5 \text{ V}$		- 5		μΑ			
lozpu		$\frac{\text{V}_{\text{CC}}}{\text{OE}} = 0 \text{ to } 1.5 \text{ V}, \text{ V}_{\text{O}} = 0.5 \text{ V to } 3 \text{ V},$ $\frac{\text{OE}}{\text{OE}} = \text{don't care}$			±100*	±100		μА		
lozpo		$\frac{\text{V}_{CC}}{\text{OE}}$ = 1.5 V to 0, V_{O} = 0.5 V to 3 V, $\frac{\text{OE}}{\text{OE}}$ = don't care			±100*		μА			
lcc		HOW HE RESERVE	Outputs high	0.19			0.19			
		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs low			5		mA		
		AI = ACC OL CIAD	Outputs disabled		0.19					
ΔlCC [‡]		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			0.2		mA			
Ci		V _I = 3 V or 0		4	4	pF				
Co		V _O = 3 V or 0		9	9	pF				

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH16240, SN74LVTH16240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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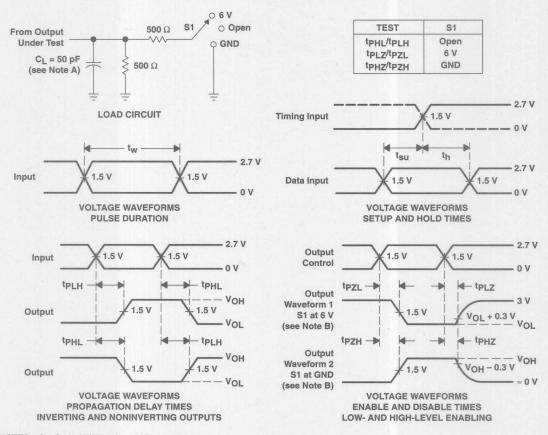
switching characteristics over recommended operating free-air temperature range, C1 = 50 pF (unless otherwise noted) (see Figure 1)

TURE CHES	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16240			SN74LVTH16240					iner.	
PARAMETER			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
tPLH	A	Υ	1	3.6	4	4.1	1	2.2	3.5		4	ns
tPHL	A		1	3.6	14	4.1	1	2.7	3.5		4	
^t PZH		Y	1	4.2	24	5.1	1	2.6	4		4.9	ns
tPZL	ŌĒ		1.1	4.6	Samo	4.8	1.2	2.6	4.4		4.6	
tPHZ	ŌĒ	Y	1.9	4.5	is = sal	5.2	2	3.4	4.5		5	ns
tPLZ	OE		1.9	44	ar e int	4.5	2	3.2	4.2		4.2	
tsk(o)‡		i an		Q Am	RE a joi			THE ST	0.5		0.5	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ Skew between any two outputs of the same package switching in the same direction

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

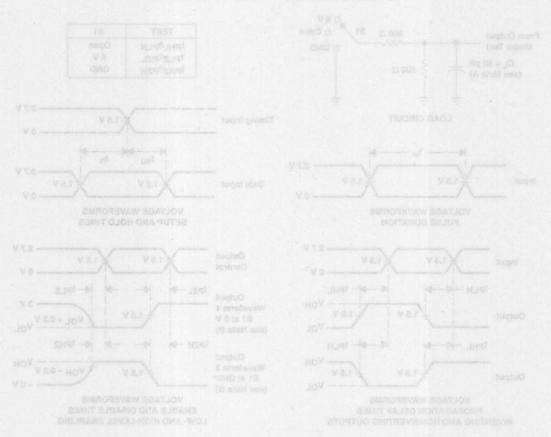
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \, \hat{\Omega}$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT RWORMATION



NOTES: A. C. Institute probe and lig expanience

- Author lugling and yet beloate perfect the supply of the supply of the output of the output of the output control of the output of the output
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 - D. The oulgula are measured one at a time with one tomerion per measuremen

Plaure 1. Lord Circuit and Voltage Waveforms



SN54LVTH162240, SN74LVTH162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

CNEAL VITHIGODAN WID DACKAGE

3Y1 13

3Y2 14

GND 15

3Y3 16

3Y4 17

VCC 18

4Y1 19

4Y2 20

GND 21

4Y3 22

4Y4 23

40E 24

36 3A1

35 3A2

34 GND

33 3A3

32 3A4

31 VCC

30 4A1

29 4A2

28 GND

27 4A3

26 4A4

25 3OE

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•	Members of the Texas Instruments Widebus™ Family	SN74LVTH162240V SN74LVTH162240DGG (TOP VIEW	OR DL PACKAGE
nveol	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation	10E 1 48	20E 7 1A1
•	Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required	blod of bs. 1Y3 5 5 44	GND 1 1A3 3 1A4
•	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})	2Y1 8 41	2 V _{CC}
•	Support Unregulated Battery Operation Bast Workship Down to 2.7 V	GND 10 39	2A2 GND
•	High-Impedance State During Power Up and Power Down		2A3 2A4

- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The 'LVTH162240 devices are 16-bit buffers/drivers designed specifically for low-voltage (3.3-V) V_{CC} operation and to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. They have the capability to provide a TTL interface to a 5-V system environment

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer and provide inverting outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

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SN54LVTH162240, SN74LVTH162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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description (continued)

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

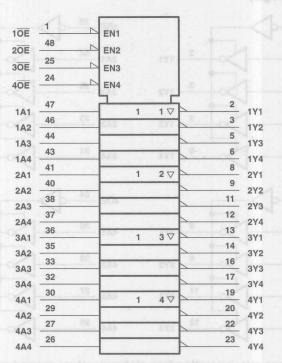
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH162240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH162240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INPL	JTS	OUTPUT
OE	Α	Y
L	Н	L (8
L	L	Н
Н	X	Z

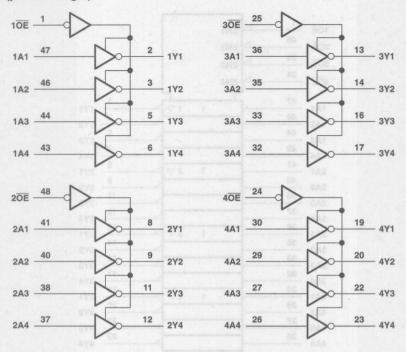
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high-impedance
or power-off state, V _O (see Note 1)
Voltage range applied to any output in the high state, VO (see Note 1)0.5 V to VCC + 0.5 V
Current into any output in the low state, IO
Current into any output in the high state, Io (see Note 2)
Input clamp current, $I_{ K }(V_{ }<0)$
Output clamp current, I _{OK} (V _O < 0)
Package thermal impedance, θ _{JA} (see Note 3): DGG package
DL package
Storage temperature range, T _{sto}

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 4)

			SN54LVTH	162240	SN74LVTH	162240	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	Voc = 8.8 V V = 20V	2.7	3.6	2.7	3.6	V
VIH	High-level input voltage	2	12	2		٧	
VIL	Low-level input voltage		0.8		0.8	٧	
VI	Input voltage	V 6	5.5	Α	5.5	V	
ЮН	High-level output current	S.A. S.A.	1 4	-12		-12	mA
loL	Low-level output current	3.6	35	12	555	12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	0	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	A STATE OF THE PROPERTY.	200		200	1 3	μs/V
TA	Operating free-air temperature	SALINE NO TRA	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DA	DAMETER	TEOT 6	CAUDITIONS	SN54LVTH16	2240	SN74	LVTH16	2240	
PA	RAMETER	TEST	CONDITIONS	MIN TYPT	MAX	MIN	TYPT	MAX	UNIT V V V μA μA μA μA μA μA μA μ
VIK		V _{CC} = 2.7 V,	I _I = -18 mA		-1.2			-1.2	V
VOH		V _{CC} = 3 V,	I _{OH} = -12 mA	2		2			V
VOL		V _{CC} = 3 V,	I _{OL} = 12 mA		0.8			0.8	V
		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V		10			10	7
1.	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND		±1			±1	A
11	D-t-1t-	V _{CC} = 3.6 V	V _I = V _{CC}	The Artist	1			MAX -1.2 0.8 10 ±1 1 -5 ±100 5 -5 ±100 0.19 5 0.19 0.2	μА
	Data inputs	ACC = 2.0 A	V _I = 0		-5			-5	
loff Vcc		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V		4			±100	μА
len en	Data inputs	V 2V	V _I = 0.8 V	75	Ü	75			^
I(hold)	hold) Data inputs VCC = 3 V		V _I = 2 V	-75		-75			μА
lozh		V _{CC} = 3.6 V,	V _O = 3 V	,Q	5			5	μΑ
lozL		V _{CC} = 3.6 V,	V _O = 0.5 V	5	-5			-5	μА
lozpu	1111	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	= 0.5 V to 3 V,	900	±100*		11.	±100	μА
IOZPD		$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = \frac{V_{CC}}{OE} = \frac{1.5 \text{ V to 0, V}_{O}}{V_{O}} = 1.5 \text{ V to 0,$	= 0.5 V to 3 V,		±100*			±100	μА
			Outputs high		0.19			0.19	
ICC		$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		5	3.7		5	mA
V		1 - VCC 01 GIVE	Outputs disabled		0.19		19413	0.19	
∆lcc [‡]		V _{CC} = 3 V to 3.6 V, Or Other inputs at V _{CC} or	ne input at V _{CC} – 0.6 V, GND		0.2		1-	0.2	mA
Ci	HARTHE !	V _I = 3 V or 0		4			4		pF
Co		V _O = 3 V or 0		9	W E		9		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.



[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH162240, SN74LVTH162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

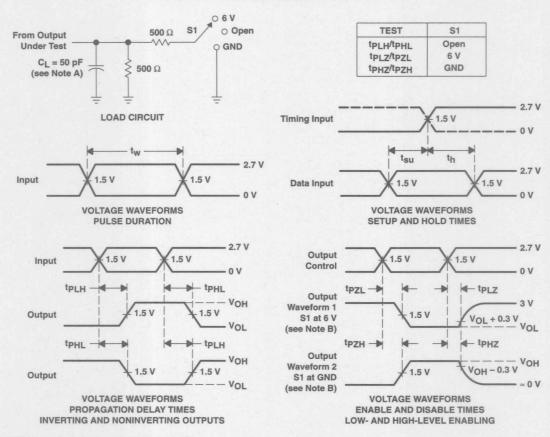
XAM		KA		S	SN54LVTH16				SN74	LVTH16	2240		
PARAMETER	FROM (INPUT)	3.6	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V		CC = 3.3 ± 0.3 V	V	V _{CC} =	2.7 V	UNIT ns ns ns
V 80		8.0		MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
tPLH	^	8.8	Y	1	4.2	4	5	1	2.5	4	spalleys	4.6	
tPHL	A	42	1	1	4.2	The same of the sa	5	1	2.9	4	so levisi-	4.6	ns
^t PZH		91	V	1	5	200	5.5	1	2.8	4.8	up level-	5.7	-
tPZL	ŌĒ	OF	1	1	4.9	3	5.1	1	2.8	4.7	Horand 2	4.9	ns
tPHZ	OE OE		Y	1.9	4.9		5.4	2	3.5	4.7	Ist du-is	5.2	VALUE OF
tPLZ	OE	50	200	1.9	47		4.8	2	3.4	4.5	ni posin	4.5	ns
tsk(o) [‡]	Tarit of value.	nells	Mine selvati teme	n Assault	Q	n artiva	Inhari uni	nice and	Veh eatt le	0.5	mione he	0.5	ns

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] Skew between any two outputs of the same package switching in the same direction

SCBS685D - MARCH 1997 - REVISED MAY 1998

PARAMETER MEASUREMENT INFORMATION

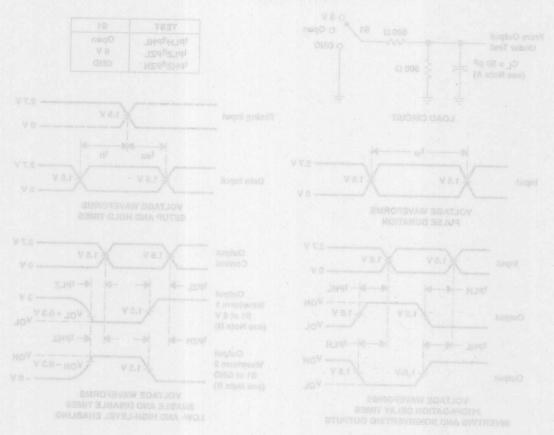


NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



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Expection 1 is for an origin with mismal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an origin with internal conditions such that the output is high except when disabled by the output control. Waveform 2 is for an original by decreated by decreated the disable of the decreated by decreated by decreated the disable of the decreated by decreated b

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Flame 1. Load Circuit and Voltage Waveforms



SN54LVTH16241, SN74LVTH16241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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•	Members of the Texas Instruments Widebus™ Family		74LVTH162	241	GG OF		
e e	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation		1Y	1 1 2 2 3	47	20E 1A1 1A2	
•	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})		GNE 1Y3	5 4 4 6	45 44	GND 1A3 1A4	
•	Support Unregulated Battery Operation Down to 2.7 V		2Y	7	41	V _{CC} 2A1	
•	High-Impedance State During Power Up and Power Down		GNE	9 10	39	2A2 GND	
•	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C		2Y4	11 12	37	2A3 2A4	
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors		GNE	1	35 34	3A1 3A2 GND 3A3	
•	Power Off Disables Outputs, Permitting Live Insertion		3Y4	4 [17	32	3A4 V _{CC}	
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise		4Y	1 19	30	4A1 4A2	
•	Flow-Through Architecture Optimizes PCB Layout			21 22		GND 4A3	
•	Latch-Up Performance Exceeds 500 mA Per JESD 17			4 [] 23 E [] 24		4A4 3OE	
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)			IAI SAI			
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings						

description

These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The devices provide noninverting outputs and complementary output-enable (OE and \overline{OE}) inputs.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

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SN54LVTH16241, SN74LVTH16241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH16241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16241 is characterized for operation from –40°C to 85°C.

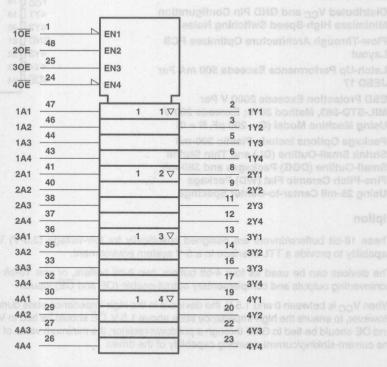
FUNCTION TABLES

INPU	TS	OUTPUTS
10E, 40E	1A, 4A	1Y, 4Y
L	Н	H
L	L	L
Н	X	Z

INPU	INPUTS					
20E, 30E 2A, 3A		2Y, 3Y				
Н	Н	Hole				
Н	L	L				
L	X	Z				

Power Off Disables Outputs, Permitting

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

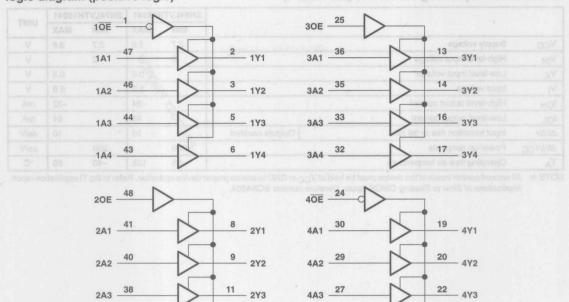
23

444

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logic diagram (positive logic)

2A4 -



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

12

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, VO (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, VO (see Note 1)	
Current into any output in the low state, IO: SN54LVTH16241	96 mA
SN74LVTH16241	
Current into any output in the high state, IO (see Note 2): SN54LVTH16241	48 mA
	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



SN54LVTH16241, SN74LVTH16241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

				SN54LVTI	116241	SN74LVT	H16241	110117
				MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage			2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage	- 1AE	191	2	12.	2		٧
VIL	Low-level input voltage			9 -	8.0		0.8	٧
VI	Input voltage	342 -45	571	40	5.5	LA2	5.5	٧
ЮН	High-level output current			4 NA	-24		-32	mA
loL	Low-level output current	86 /00		25	48	200	64	mA
Δt/Δv	Input transition rise or fall rate		Outputs enabled	0	10	9.1510	10	ns/V
Δt/ΔVCC	Power-up ramp rate	96	a	200		200	i m	μs/V
TA	Operating free-air temperature			-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETED IN	THE CONTRACT OF THE CONTRACT O	L. Lower Herry Jackson	SN54LVTH1	6241	SN74LVTH16	6241		
PAI	RAMETER	TEST C	ONDITIONS	MIN TYPT	MAX	MIN TYPT	MAX	UNIT	
VIK	A 100 = 000 a	V _{CC} = 2.7 V,	I _I = -18 mA	O THAT	-1.2	(HPUT)	-1.2	٧	
	MIN MAX	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.2		V _{CC} -0.2			
.,		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4		2.4	+	J91 _V	
VOH		V 0.V	I _{OH} = -24 mA	2				Hat	
		VCC = 3 V	I _{OH} = -32 mA	11		2			
211	4.8	V 0.7.V	I _{OL} = 100 μA	1	0.2	30 10 50	0.2	tpg	
		V _{CC} = 2.7 V	I _{OL} = 24 mA	91	0.5		0.5		
V		2 34 49	I _{OL} = 16 mA	81	0.4	BO 10 SU	0.4	V	
VOL		V 2V	I _{OL} = 32 mA		0.5		0.5	plat	
		V _{CC} = 3 V	I _{OL} = 48 mA	Oras	0.55	S.E street Vita etc	equiav l	il typica	
			I _{OL} = 64 mA	padatiwe egistore	othing onl	to anutino out y	0.55		
		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V		\$ 10		10		
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Š	±1		±1		
lį		Vcc = 3.6 V	V _I = V _{CC}	- DE	1		1.	μА	
Data inputs		ACC = 2.0 A	V _I = 0	1	-5				
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V	250	±100		±100	μΑ	
lea es	Data inputs	V2V	V _I = 0.8 V	750	MEET A	75		μА	
I(hold)	Data inputs	VCC = 3 V	V _I = 2 V	-75		-75		μА	
IOZH		V _{CC} = 3.6 V,	V _O = 3 V		5		5	μΑ	
lozL		V _{CC} = 3.6 V,	V _O = 0.5 V		-5		-5	μΑ	
lozpu		$V_{CC} = 0$ to 1.5 V, $V_{O} = 0$ OE/OE = don't care	0.5 V to 3 V,		±100*		±100	μА	
IOZPD		V _{CC} = 1.5 V to 0, V _O = OE/OE = don't care	= 0.5 V to 3 V,		±100*		±100	μА	
			Outputs high		0.19		0.19		
lcc		$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		5		5	mA	
		AI - ACC OLGIND	Outputs disabled		0.19	0.19			
ΔICC [‡]		V _{CC} = 3 V to 3.6 V, On Other inputs at V _{CC} or	e input at V _{CC} - 0.6 V, GND		0.2		0.2	mA	
Ci		V _I = 3 V or 0		4		4		pF	
Co		V _O = 3 V or 0		9		9		pF	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH16241, SN74LVTH16241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

TINU	SN74LVTH16	PASHPHTVARE		SN54LV	TH16241	arridue	SN74LVTH16241					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		2.7 V VCC = 3.3 V ± 0.3 V		V	V _{CC} = 2.7 V		UNIT
	Voc-0.2	2.0	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
t _{PLH}	A		1.1	3.7	Am &	4	1.2	2.6	3.5		3.8	200
t _{PHL}	A	Y	1.1	3.7	ATTU	- 4	1.2	2.2	3.5		3.8	ns
^t PZH	- SE - SE	V	1.1	4.7	44	5.3	1.2	3.2	4.5		5.1	no
tPZL	OE or OE	2.0	1.1	4.7	Xu 091	5.2	1.2	3.2	4.5		4.9	ns
tPHZ		00 V	1.9	5.5	24 mA	6.1	2	3.7	5.3		5.9	
tPLZ	OE or OE	4.0	1.9	5.2	Am 81	5.7	2	3.4	4.9		5.4	ns
tsk(o) [‡]		5.0		Q"	Am St	# JO!		100	0.5		0.5	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

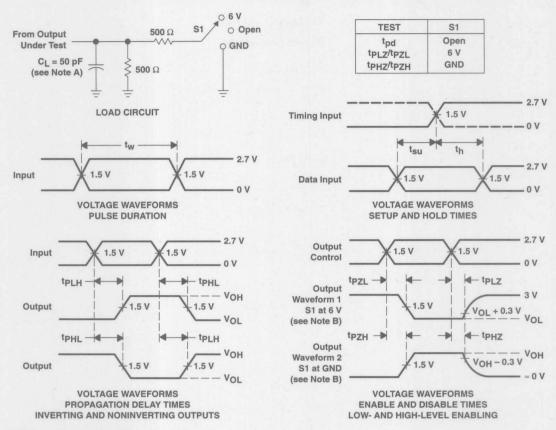
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



[‡] Skew between any two outputs of the same package switching in the same direction

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PARAMETER MEASUREMENT INFORMATION

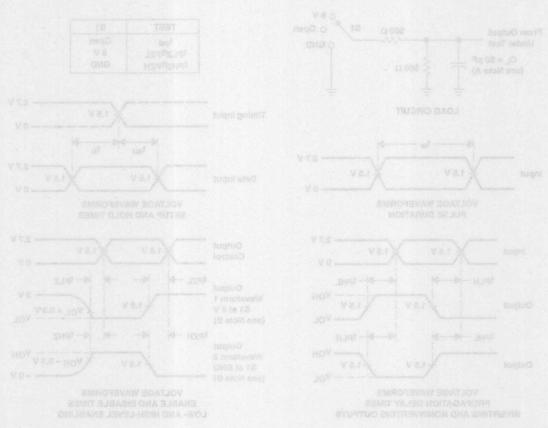


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \, \Omega$, $t_{f} \leq 2.5 \, \text{ns}$, $t_{f} \leq 2.5 \, \text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Cr Includes probe and jip capacitance

Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is fer an output with internal conditions attent in output is high except when disabled by the output control.
 Waveform 2 is fer an output with internal condition has believed in output is high except which size output control.

D. The outputs are measured one of a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Wavelorms



SN54LVTH162241, SN74LVTH162241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS692C - MAY 1997 - REVISED MAY 1998

•	Members of the Texas Instruments Widebus™ Family	SN		1		PACKAGE R DL PACKAGE
or and	Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required		10E [1	48	20E
sietor ad by	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation		1Y2 [GND [1Y3 [1Y4 [3 4 5	46 45	1A2 GND 1A3
.o*es	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})		2Y2 [8	42 41 40	00
•	Support Unregulated Battery Operation Down to 2.7 V		GND [11	38	GND 2A3
•	and Power Down		3Y1 L	13	36	2A4 3A1
•	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C		3Y2 [GND [3Y3 [15	34	3A2 GND 3A3
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors		3Y4 [V _{CC} [17 18	32 31	3A4
•	Power Off Disables Outputs, Permitting Live Insertion		4Y2 [GND [20	29	4A2 GND
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise		4Y3 [4Y4 [23	26	4A3 4A4
•	Flow-Through Architecture Optimizes PCB Layout		40E [24	25	30E

JESD 17

• ESD Protection Exceeds 2000 V Per

Latch-Up Performance Exceeds 500 mA Per

- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The devices provide noninverting outputs and complementary output-enable (OE and \overline{OE}) inputs.

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SN54LVTH162241, SN74LVTH162241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS692C - MAY 1997 - REVISED MAY 1998

description (continued)

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH162241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH162241 is characterized for operation from –40°C to 85°C.

FUNCTION TABLES TO THE TABLE SEAL DOWN THE THE TABLES

INPU	OUTPUTS	
10E, 40E	1A, 4A	1Y, 4Y
L	Н	Н
L	L	Leon
Н	X	Z

INPU	OUTPUTS			
20E, 30E	2A, 3A	2Y, 3Y		
Н	Н	Н		
Н	L	L		
L	X	Z		

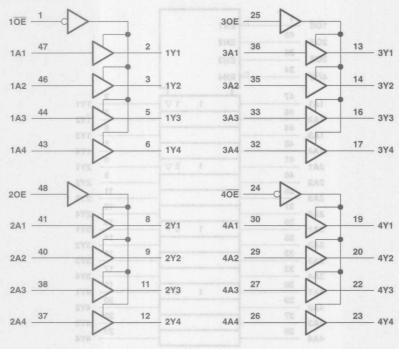
logic symbol†

	1	28						
10E	48		EN1					
20E	25	0.0	EN2		1Ver			
30E	-		EN3		2001			
40E	24		EN4					
	47		7	_			2	
1A1	46	33		1	1 ▽	8	3	1
1A2	44		Day O		0.00		5	1
1A3 1A4	43	92			571	a	6	1
	41			1	2.77		8	
2A1	40		-	-	2 ▽		9	2
2A2	38	45	EO5				11	2
2A3	37						12	2
2A4	36	06	FAR	_	3 ▽	8	13	2
3A1	35		-	1	3 ∨		14	3
3A2	33	98	045		eve	N.	16	3
3A3	32						17	3
3A4	30	27	242		457	41	19	3
4A1	29			1	4 ▽		20	4
4A2	27	- 25	200		2.46	SP	22	4
4A3	26		-		1112		23	4
4A4				5.5		D. 77		4

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, VO (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, VO (see Note 1)	
Current into any output in the low state, IO	30 mA
Current into any output in the high state, IO (see Note 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, IOK (VO < 0)	
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

This current flows only when the output is in the high state and V_O > V_{CC}.
 The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4) a believe the solid halos and a grid of

		A SOUTH		SN54LVTH	162241	SN74LVTH	1162241	LIMIT
				MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	Luce-	V 6.6 = 30V	2.7	3.6	MOT 2.7	3.6	٧
VIH	High-level input voltage		F 0.3 A	2	12	2		V
VIL	Low-level input voltage	AAM	WIN MAX WIN		0.8		0.8	٧
VI	Input voltage	84 /	5,6 8.1	I v	5.5	A	5.5	V
ЮН	High-level output current	8.0	19 9 feet	1	-12		-12	mA
loL	Low-level output current	8.8	30 24 11	35	12	20 m 30	12	mA
Δt/Δν	Input transition rise or fall rate	A.B.	Outputs enabled	0	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	12.0	16,0 0.7	200		200	7 2	μs/V
TA	Operating free-air temperature	1.0	36 61	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				SN54	LVTH16	2241	SN74	LVTH16	2241	UNIT
PAI	RAMETER	TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	V
Vон		V _{CC} = 3 V,	I _{OH} = -12 mA	2		1	2			V
VOL		V _{CC} = 3 V,	I _{OL} = 12 mA			0.8			0.8	V
		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10			10	
1.	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND		V.	±1		5	±1	μА
li .		puts V _{CC} = 3.6 V	V _I = V _{CC}			1			1	μА
	Data inputs		V _I = 0			-5			-5	
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V			±100			±100	μΑ
lia ia	Data inputs	V2V	V _I = 0.8 V	75	4	Q I	75			^
I(hold) Data inputs		VCC = 3 V	V ₁ = 2 V	-75	W.		-75			μА
lozh		V _{CC} = 3.6 V,	V _O = 3 V		,0	5			5	μΑ
lozL		V _{CC} = 3.6 V,	V _O = 0.5 V		O.	-5			-5	μΑ
lozpu		$V_{CC} = 0$ to 1.5 V, $V_{O} = 0$	0.5 V to 3 V,	0	7	±100*			±100	μА
IOZPD		V _{CC} = 1.5 V to 0, V _O = OE/OE = don't care	0.5 V to 3 V,			±100*			±100	μА
			Outputs high			0.19	7		0.19	
Icc		$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low			5	5		mA	
		AI - ACC OL CIAD	Outputs disabled		The s	0.19	0.19			
Δlcc [‡]		V _{CC} = 3 V to 3.6 V, One Other inputs at V _{CC} or	e input at V _{CC} - 0.6 V, GND			0.2			0.2	mA
Ci		V _I = 3 V or 0			4		The same	4		pF
Co		V _O = 3 V or 0			9			9		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

 $^{^{\}dagger}$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVTH162241, SN74LVTH162241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

THU XAM		MAX		S	N54LVT	H162241			SN74	LVTH16	2241			
PARAMETER	FROM (INPUT)	3.8	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	Vo	C = 3.3 ± 0.3 V	V	V _{CC} =	2.7 V	UNIT	
v láo		8.0		MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	(
tPLH	Δ.	a.a ~	Y	1.3	4.3	12.	4.9	1.4	3	4.1	kosticy t	4.7		
tPHL	A		T T	1.3	4.3	34	4.9	1.4	2.4	4.1	in invel	4.7	ns	
^t PZH	OF 0F	12	Y	1.1	5.2	Q.	5.9	1.2	3.5	4.9	oc level	5.7	ns	
tPZL .	OE or OE	07		1.4	5	Soll	5.4	1.5	3.5	4.8	thanath	5.2	IIS	
tPHZ	OE or OE		V.	1.9	5.5		6.2	2	3.7	5.3	en dunien	5.9	ns	
tPLZ	OE or OE	201	22.	1.9	5.2		5.7	2	3.6	4.9	st neites	5.4	ns	
tsk(o) [‡]	Feder with a	nois a	son enimely suppri	V discounted	Q.	nion 17 lis	below to med	beam only	enia escit la	0.5	offeren his	0.5	ns	

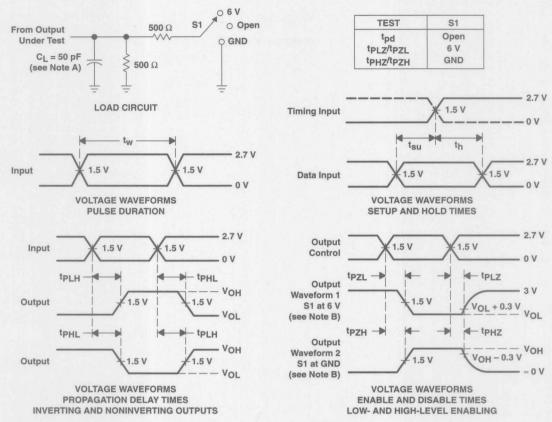
[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] Skew between any two outputs of the same package switching in the same direction

			8		

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PARAMETER MEASUREMENT INFORMATION

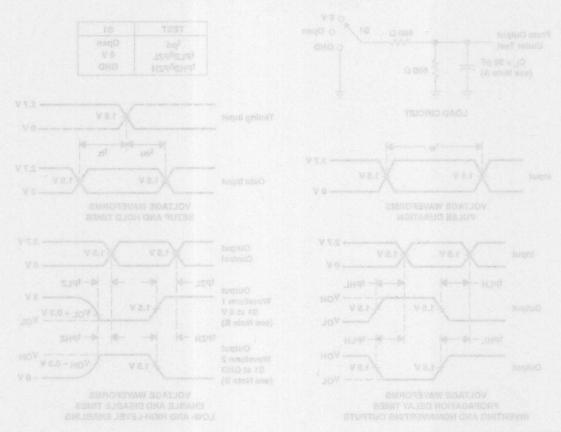


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \, \Omega$, $t_{f} \leq 2.5 \, \text{ns}$, $t_{f} \leq 2.5 \, \text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Og Includes probe and lig capacitano
- Waveform 1 is for an output with infernal conditions such that the output is low sidest when disabled by the output control.
 Waveform 2 is for an output with infernal conditions such that the output social when disabled by the output control.
- All input pulses are supplied by generators having the following obstaclaristics: PRR ≤ 10 MHz, Z_O ≥ 50 Ω, f_i ≤ 2.5 ns, f_i ≤ 2.5 ns
 - 2. The outputs are mensured one at a time with one transition per measurement.

Floure 1, Load Circuit and Voltage Waveforms



SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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•	Widebus™ Family		SN74LVTH16244A.		. WD PACKAGE DGV, OR DL PACKAGE EW)
•	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation		10E 1Y1 1Y2	1 2	48 20E 47 1A1 46 1A2
•	High-Impedance State During Power Up and Power Down		GND 1Y3	4	45 GND 44 1 1A3
•	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V VCC)		1Y4 Vcc 2Y1	6 7 8	43 1 1A4 42 1 V _{CC} 41 1 2A1 40 1 2A2
•	Support Unregulated Battery Operation Down to 2.7 V		GND	10	39 GND
•	Typical V _{OLP} (Output Ground Bounce) $< 0.8 \text{ V}$ at V _{CC} = 3.3 V, T _A = 25°C		2Y4	12	38 2A3 37 2A4
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors		3Y1 3Y2 GND	14 15	36 3A1 35 3A2 34 GND
•	Power Off Disables Outputs, Permitting Live Insertion		3Y3 3Y4	17	33 3A3 32 3A4 31 V _{CC}
•	Latch-Up Performance Exceeds 500 mA F JESD 17	Per	V _{CC} 4Y1 4Y2	19	30 4A1 29 4A2
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 Using Machine Model (C = 200 pF, R = 0)	V	GND 4Y3 4Y4	21 22	28 GND 27 4A3 26 4A4
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-m Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings	nil	4 0 E	ic is	25 3 0E

description

The 'LVTH16244A devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5-V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5-V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16244A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVTH16244A is characterized for operation from -40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated.



FUNCTION TABLE (each buffer)

INPL	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	X	Z

logic symbol†

					1
	- 1		EN1		48
			EN2		25
			EN3		24
			EN4		24
		_			47
3 1Y2	1 🗸 –	1	_		46
5 1Y3		_			44
6 1Y4	_			ring !	43
8 2Y1	2 🗸	-			41
9 272	2 ∨	1	-		40
11 2Y3					38
12	4.0				37
13 3Y1	3 ▽ -	1		101.13	36
14	3 V	1			35
16		_			33
17 3Y4	There d			Far II	32
19 4Y1	4 🗸 –	1			30
20 4Y2	4 *	-			29
22 4Y3					27
23 474					26

Members of the Texas Instruments

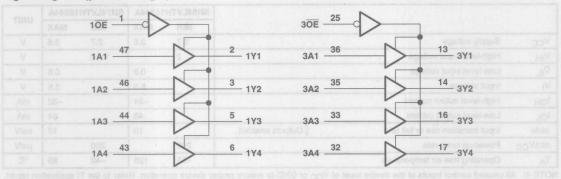
High-impedance State During Power

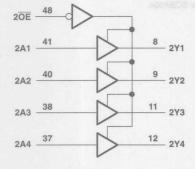
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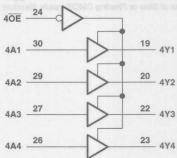
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high-impedance
or power-off state, V _O (see Note 1)
Voltage range applied to any output in the high state, V_O (see Note 1)0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, Io: SN54LVTH16244A
SN74LVTH16244A
Current into any output in the high state, I _O (see Note 2): SN54LVTH16244A
SN74LVTH16244A
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0)
Package thermal impedance, θ _{JA} (see Note 3): DGG package
DGV package 93°C/W
DL package
Storage temperature range, T _{stg}

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

3. The package thermal impedance is calculated in accordance with JESD 51.



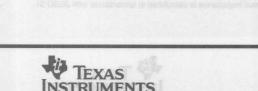
SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS142K - MAY 1992 - REVISED MARCH 1998

recommended operating conditions (see Note 4)

		-		SN54LVTH	16244A	SN74LVTH	16244A	111117
				MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage			2.7	3.6	2.7	3.6	V
VIH	High-level input voltage	TAE	171	2		2	51.51	٧
VIL	Low-level input voltage			-	0.8		0.8	V
VI	Input voltage	3AS	5Y1 - E	11/1	5.5	SAT	5.5	V
ЮН	High-level output current				-24		-32	mA
loL	Low-level output current	86 PAR	ALC: 1		48	55 000	64	mA
Δt/Δν	Input transition rise or fall rate	O	utputs enabled		10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	92		200	4	200		μs/V
TA	Operating free-air temperature				125	-40	85	°C

NOTE 4: All unused control inputs of the device must at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS142K - MAY 1992 - REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

-	Abbs	SHTVLIATHE	SHEALVTHIESKED	SN54LVTH16244A	SN74LVTH16244/	Α
PARAMETER		TEST CON	IDITIONS	MIN TYPT MAX	MIN TYPT M	AX UNI
VIK	1	V _{CC} = 2.7 V,	I _I = -18 mA	-1.2	(FUNNI)	1.2 V
	MIN MAK	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.2	V _{CC} -0.2	
		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	2.4	[H] [H]
VOH		2.8 2 8.1 19	I _{OH} = -24 mA	2		V
		VCC = 3 V	I _{OH} = -32 mA	L. v	2	HEST
	10	111 0 0011	I _{OL} = 100 μA	0.2		0.2
		V _{CC} = 2.7 V	I _{OL} = 24 mA	0.5	55	0.5
		2 3.1 4.2	I _{OL} = 16 mA	0.4		0.4
VOL		8.0	I _{OL} = 32 mA	0.5		0.5 V
		VCC = 3 V	I _{OL} = 48 mA	0.55	/ E.S = 3:3V Is etc aau	typical val
		E White the state of the state	I _{OL} = 64 mA	Lithus afterned aums er	0	.55
		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	50		10
l.	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	±1	- 12 Tay - 1	±1 μΑ
l _l	D-4-14-	V _{CC} = 3.6 V	V _I = V _{CC}	1		1 μΑ
	Data inputs	VCC = 3.0 V	V _I = 0	-5		-5
loff		$V_{CC} = 0$, V_I or $V_O = 0$ to 4	1.5 V		±1	00 μΑ
Ira r.s	Data inputs	V _{CC} = 3 V	V _I = 0.8 V	75	75	μА
I(hold)	Data Inputs	vCC = 3 v	V _I = 2 V	-75 -75		μА
lozh		V _{CC} = 3.6 V,	$= 3.6 \text{ V}, \qquad \qquad \text{V}_{\text{O}} = 3 \text{ V}$			5 μΑ
lozL		V _{CC} = 3.6 V,	$V_0 = 0.5 V$	-5		–5 μA
lozpu		$\frac{V_{CC}}{OE}$ = 0 to 1.5 V, V_{O} = 0.5 V to 3 V, OE = don't care		±100*	±1	00 μΑ
IOZPD		$\frac{\text{V}_{CC}}{\text{OE}} = 1.5 \text{ V to 0, V}_{O} = 0.5 \text{ V}_{O}$	5 V to 3 V,	±100*		00 μΑ
		V 00VI 6	Outputs high	0.19	0	.19
lcc		$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low	5	TREE TREE TO THE	5 mA
		1 700 01 0110	Outputs disabled	0.19	0	.19
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2 mA
Ci		V _I = 3 V or 0		4	4	pF
Co		V _O = 3 V or 0		9	9	pF

^{*}On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

† This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS142K - MAY 1992 - REVISED MARCH 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

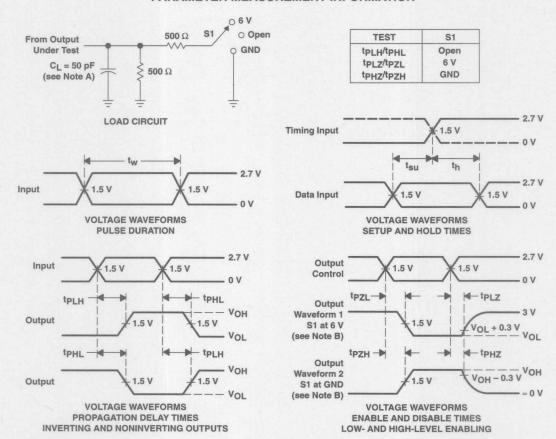
ANDS	FROM (INPUT)	то (оитрит)	S	SN54LVTH16244A			SN74LVTH16244A					
PARAMETER			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
t _{PLH}	A		1.1	4.4	le main	4.6	1.2	2.3	3.2		3.7	
tPHL	A	Y	1.1	3.6	in a Live	3.9	1.2	2	3.2		3.7	ns
t _{PZH}			1.1	4.6	in a narry	5.4	1.2	2.6	4		5	
tPZL	ŌĒ	1.0	1.1	5.4	ot a rol	6.2	1.2	2.7	4		5	ns
tPHZ		10 4	1.6	5.7	is a and	6.2	2.2	3.3	4.5		5	
tPLZ	ŌĒ	10	1.2	5	1 m	4.7	2	3.1	4.2		4.4	ns
tsk(o)‡		5.0		Am	SB = 101				0.5			ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ Skew between any two outputs of the same package switching in the same direction

	VOC = 1.5 V to 0, VO = 0.5 V to 3 V.				

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PARAMETER MEASUREMENT INFORMATION

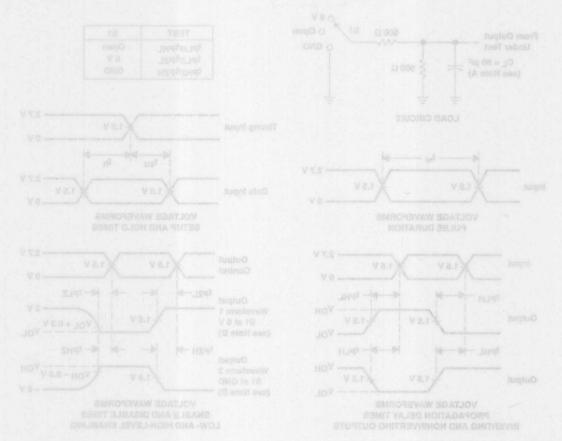


NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \,\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C. includes probe and lig capacitance

B. Wavetone 1 is for an output with entenal conditions such that the output is high except when disabled by the output control. Wavetonn 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All frout outputs as an excepted by operations having the following characteristics: PRR ≤ 10 MHz. Zn = 50 Ω Ω t ≤ 2.5 ns. t ≤ 2.5 ns.

The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTSWITH 3-STATE OUTPUTS

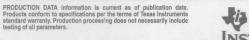
SCBS258I - JUNE 1993 - REVISED MARCH 1998

•	Members of the Texas Instruments Widebus™ Family	SN74LVTH16224	41	WD PACKAGE DGG OR DL PACKA VIEW)	GE
.mwo	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation	10E (1 2	48 20E 47 1A1 46 1A2	
100	Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required	GND 11/3	4 5	45 GND 44 11A3 43 1A4	
•	Cumpart Mixed Made Cianal Operation	V _{CC} 2Y1 2Y2	8	42 V _{CC} 41 2A1 40 2A2	
•	Support Unregulated Battery Operation Down to 2.7 V	GND 2Y3	11	39 GND 38 2A3	
•	High-Impedance State During Power Up and Power Down	3V1	13	37 2A4 36 3A1 35 3A2	
•	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C	GND	15	34 GND 33 3A3	
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors	3Y4 V _{CC} 4Y1	17 18	32 3A4 31 V _{CC} 30 4A1	
•	Power Off Disables Outputs, Permitting Live Insertion	4Y2	20	29 4A2 28 GND	
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise	4Y3 4Y4	23	27 4A3 26 4A4	
•	Flow-Through Architecture Optimizes PCB Layout	40E	24	25 3OE	
•	Latch-Up Performance Exceeds 500 mA Per JESD 17				
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)				
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings				

The 'LVTH162244 devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

Widebus is a trademark of Texas Instruments Incorporated.

description





SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTSWITH 3-STATE OUTPUTS

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description (continued)

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

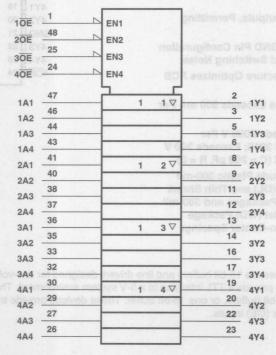
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH162244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH162244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INP	JTS	OUTPUT
OE	Α	Ygu
L	Н	Н
L	L	L ()
Н	X	Z

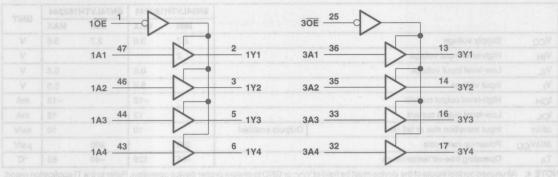
logic symbol†

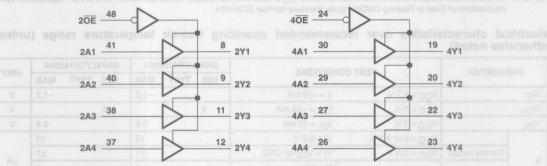


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCBS258I - JUNE 1993 - REVISED MARCH 1998

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	Supply voltage range, V _{CC}	0.5 V to 4.6 V
	Input voltage range, V _I (see Note 1)	
	Voltage range applied to any output in the high-impedance	
	or power-off state, V _O (see Note 1)	0.5 V to 7 V
Ac	Voltage range applied to any output in the high state, VO (see Note 1) .	
. (Current into any output in the low state, IO	V
(Current into any output in the high state, IO (see Note 2)	30 mA
	Input clamp current, I _{IK} (V _I < 0)	
	Output clamp current, IOK (VO < 0)	
	Package thermal impedance, θ Δ (see Note 3): DGG package	89°C/W
	DL package	94°C/W
	Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This current flows only when the output is in the high state and $V_O > V_{CC}$.

^{3.} The package thermal impedance is calculated in accordance with JESD 51.

SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTSWITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

	MINISTER STATE OF THE STATE OF	30	SN54LVTH	1162244	SN74LVTH	162244	LINUS
			MIN	MAX	MIN	MAX	0 UNIT 0 V V V V V V V V V V V V V V V V V V
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage	1Y1 3A1	2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage	172 302		5.5	TAZ	5.5	V
ЮН	High-level output current		6	-12		-12	mA
loL	Low-level output current	EB PAR CYT.		12	AL MAY	12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	50 32	200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER	TEOT	ONDITIONS	TONS SN54LVTH162244 SN74LVTH162244		2244	UNIT				
PAI	RAMETER	IESI C	ONDITIONS	MIN	TYPT	MAX	MIN TYPT MAX		UNIT		
VIK		V _{CC} = 2.7 V,	$I_{\parallel} = -18 \text{ mA}$			-1.2			-1.2	٧	
Vон	-	V _{CC} = 3 V, I _{OH} = -12 mA		2	-		2			V	
VOL		V _{CC} = 3 V,	I _{OL} = 12 mA	1 3 3		0.8			0.8	V	
	2111111	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	12	1	10	76		10		
6.	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1		PAL	±1	μА	
l _l		V _{CC} = 3.6 V	V _I = V _{CC}			1.			1	μА	
†(beix	Data inputs	ACC = 2.0 A	V _I = 0	anites	eco re	-5	nlten i	numb	-5	ulos	
loff		$V_{CC} = 0$,	V_{1} or $V_{0} = 0$ to 4.5 V					A DEE	±100	μΑ	
lon on	A inputs	V _{CC} = 3 V	V _I = 0.8 V	75		00	75	a epan	on Aide	μА	
I(hold)	Amputs	ACC = 2 A	V _I = 2 V	-75	(F. SIG	M GIRC'	-75	age ren	alma to	μА	
lozh	/an	V _{CC} = 3.6 V,	V _O = 3 V	P COLUMN	r ainis	5	V atat	arya cq. arvolf e	5	μА	
IOZL	99 V 10 Vee	V _{CC} = 3.6 V,	V _O = 0.5 V	of the blo	d fraction	-5	hellor	is spa	-5	μА	
lozpu		$\frac{V_{CC}}{OE} = 0 \text{ to } 1.5 \text{ V, V}_{O} = 0$	0.5 V to 3 V,	±100*			tuquo yas off ±100			μА	
lozpd		$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = \frac{V_{CC}}{OE} = \text{don't care}$	0.5 V to 3 V,	±100*) NI JITEMUS QT ±100			μА	
VAD RE			Outputs high	e Note	92) A 8	0.19	impe	emedi	0.19	99	
loc		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs low			5			5	mA	
		1 1 - 1 CC of and	Outputs disabled		· · · · · · · ·	0.19	n enun	enagme	0.19		
Δlcc [‡]	are stress ratings perating condition	V _{CC} = 3 V to 3.6 V, One Other inputs at V _{CC} or		griller mp Baco serb	e maxim or any o	0.2	ebnu be epiveb :	tell asorti on of the	0.2	mA	
Ci		V _I = 3 V or 0	extended pariods may allect	ol scotti	4	gr-mumi	em alui	4	преде	pF	
Co	SERVICE OF SPICIES	V _O = 3 V or 0	grade exceptional a use a grade of	I SUNDA	9	SAMPLE OF	Hapter 1	9	Will to	pF	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

† This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTSWITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

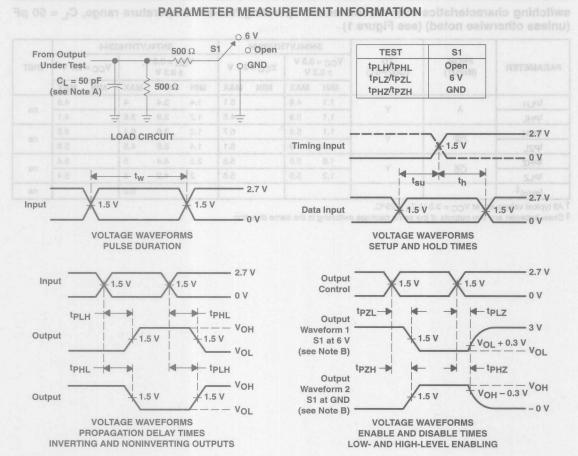
		1037	S	N54LVT	H162244	1 3		SN74	LVTH16	2244		
PARAMETER	RAMETER (INPUT) (OUT	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} =	2.7 V	UNIT	
		1000fested	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
t _{PLH}		Y	1.1	4.6		5.1	1.4	3.4	4		4.8	
tPHL	Α	T	1.1	3.9		4.5	1.2	2.9	3.6		4.1	ns
V ^t PZH			1.1	5.4		6.7	1.2	3.9	5.1	pile .	6.5	
tPZL	ŌĒ	T	1.3	4.9		6.1	1.4	3.8	4.5		5.8	ns
tPHZ	A name once once other?	V	1.6	5.5		5.8	2.2	4.4	5		5.4	
tPLZ	ŌĒ	al Y	1.2	5.9		5.8	2	4.2	5		5.4	ns
tsk(o) [‡]					VY.	T rotation		/	0.5		,	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



[‡] Skew between any two outputs of the same package switching in the same direction

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NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \, ns$, $t_f \leq 2.5 \, ns$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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•	Members of the Texas Instruments <i>Widebus</i> ™ Family	and the same of th	H16245A	. DGG	WD PACKAGE , DGV, OR DL PACKAGE	
Stor	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power		1DIR		48 10E	
	Dissipation and how static rower		1B1 L	541 0.201	47 1A1	
	High-Impedance State During Power Up		1B2 GND		46 1 1A2 45 1 GND	
	and Power Down		1B3 [44 1 1A3	
	Support Mixed-Mode Signal Operation		1B4 [43 1 1A4	
	(5-V Input and Output Voltages With		V _{CC} [42 VCC	
	3.3-V Voc) HOITARERO		1B5 [41 1A5	
	Support Unregulated Battery Operation		1B6 [9	40 1A6	
	Down to 2.7 V	4 - 4 1	GND [10	39 GND	
	Distributed V _{CC} and GND Pin Configuration		1B7 [11	38 1A7	
	Minimizes High-Speed Switching Noise		1B8 [12	37 1A8	
	Flow-Through Architecture Optimizes PCB		2B1	13	36 2A1	
	Layout		2B2		35 2A2	
			GND		34 GND	
	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C		2B3	1	33 2A3	
	PROPERTY AND ADDRESS OF THE PROPERTY A		2B4		32 2A4	
	Bus Hold on Data Inputs Eliminates the		Vcc		31 V _{CC}	
	Need for External Pullup/Pulldown Resistors		2B5 L		30 2A5	
			2B6		29 2A6	
	Tower on Disables outputs, Termitting		GND L 2B7		28 GND 27 2A7	
		-	2B7 L		26 2A8	
•	Latch-Up Performance Exceeds 500 mA Per JESD 17	TV-	2DIR [25 2 0 E	
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)					
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package					
	Using 25-mil Center-to-Center Spacings					

description

The 'LVTH16245A devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated



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description (continued)

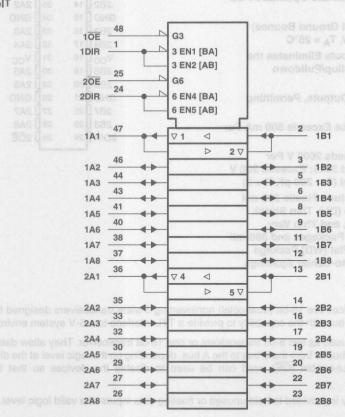
When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16245A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16245A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

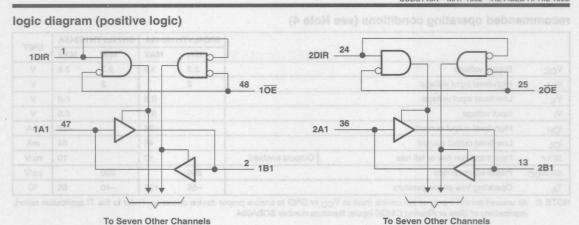
INP	UTS	ODEDATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}
Voltage range applied to any output in the high-impedance
or power-off state, V _O (see Note 1)
Voltage range applied to any output in the high state, V _O (see Note 1) −0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, Io: SN54LVTH16245A
SN74LVTH16245A
Current into any output in the high state, I _O (see Note 2): SN54LVTH16245A
SN74LVTH16245A
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0)50 mA
Package thermal impedance, $\theta_{\rm JA}$ (see Note 3): DGG package
DGV package
DL package
Storage temperature range, T _{stg} 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and $V_O > V_{CC}$. 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

			SN54LVTH	16245A	SN74LVTH	16245A	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
V _{IH}	High-level input voltage	16 100	2		2		V
VIL	Low-level input voltage			0.8	10,110	0.8	٧
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current	243 26		-24	<	-32	mA
loL	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	N.	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	181	200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

TEXAS INSTRUMENTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	SASSA	HIND THE CONTROL OF T	SAUGALYTHIS SAUGA	SN54	LVTH16	245A	SN74LVT	H16245A	LIBUT	
PA	RAMETER	V S.M = DOV	ONDITIONS		TYPT		MIN	PT MAX	UNIT	
VIK		V _{CC} = 2.7 V,	I _I = -18 mA	0 3	(10910	-1.2	(EUPPUS)	-1.2	٧	
	XAM MINI	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0	.2		V _{CC} -0.2			
		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	E so E		2.4	H	V	
VOH		1.8 2.1	I _{OH} = -24 mA	2					A LEEP	
		VCC = 3 V	I _{OH} = -32 mA	22	8 10 /		2	1	(4)	
	5.2	V 0.7 V	I _{OL} = 100 μA	6.12		0.2		0.2	[g]	
		V _{CC} = 2.7 V	I _{OL} = 24 mA		B 10 A	0.5	55	0.5	foli	
		2.2 3.5 6	I _{OL} = 16 mA			0.4		0.4	jej V	
VOL		O O V	I _{OL} = 32 mA			0.5		0.5	V	
		V _{CC} = 3 V	I _{OL} = 48 mA		2570.	0.55	6 = 00 V 18	d values are a	All typical	
			I _{OL} = 64 mA	AID SUDWED	invest i	Huma sau	to sindino ni	0.55	SE WANK	
	Controllinguite	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1		±1		
	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10		10		
lį		WILL TO US STORE	V _I = 5.5 V			20		20	μА	
	A or B ports‡	V _{CC} = 3.6 V	V _I = V _{CC}			5		1		
			V _I = 0			-5		-5		
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V					±100	μΑ	
lea es	A or B ports	V _{CC} = 3 V	V _I = 0.8 V	75	51.33.0		75	- J	μА	
I(hold)	A of B ports	ACC = 2 A	V _I = 2 V	-75			-75		μА	
lozpu		$\frac{V_{CC}}{OE} = 0 \text{ to } 1.5 \text{ V, V}_{O} = 0$	= 0.5 V to 3 V,			±100*		±100	μА	
lozpd		$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = 1.5 V to $	= 0.5 V to 3 V,			±100*		±100	μА	
		V _{CC} = 3.6 V,	Outputs high			0.19		0.19		
ICC§		$I_0 = 0$,	Outputs low			5		5	mA	
		V _I = V _{CC} or GND	Outputs disabled			0.19		0.19		
Δlcc		V _{CC} = 3 V to 3.6, One Other inputs at V _{CC} or				0.2		0.2	mA	
Ci	10.44,250/17	V _I = 3 V or 0			4			4	pF	
Cio		V _O = 3 V or 0			10	10,1		10	pF	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25° C. ‡ Unused pins at V_{CC} or GND

^{\$} This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

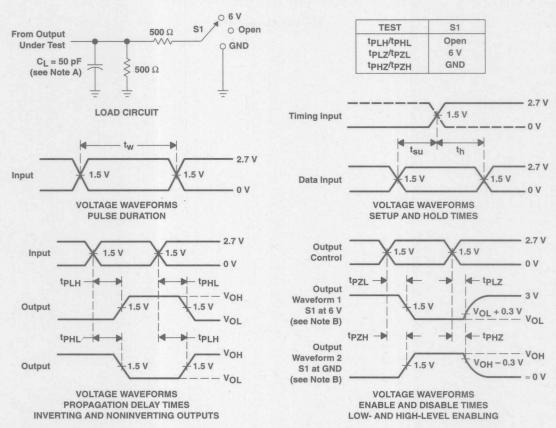
ABAS		ABASSTHTVJAS	S	N54LVT	H16245/	4		SN74	LVTH16	245A	white a	
PARAMETER	FROM (INPUT)	TO (OUTPUT)				CC = 3.3 ± 0.3 V	V	V _{CC} =	2.7 V	UNIT		
		5.0	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	N MAX	
tPLH	A or B	B or A	0.5	4.5	Am Boo	4.6	1.5	2.3	3.3	25.33	3.7	
tPHL	AOIB	BOLA	0.5	4.4	am NS-	3.9	1.3	2.1	3.3		3.5	ns
^t PZH	ŌĒ	A or B	0.5	6.5	Nm 58-	6.6	1.5	2.8	4.5		5.3	
tPZL	OE	AOIB	0.5	5.4	700 u.K	6.2	1.6	2.9	4.6		5.2	ns
tPHZ	ŌĒ	A or B	1	6.8	Am AS	7	2.3	3.7	5.1	R. Live	5.5	
tPLZ	OE	AOIB	1	6.2	Am at	6.3	2.2	3.5	5.1		5.4	ns
tsk(o)‡	Made	Lo			Am SB	5 107			0.5		0.5	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] Skew between any two outputs of the same package switching in the same direction

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PARAMETER MEASUREMENT INFORMATION



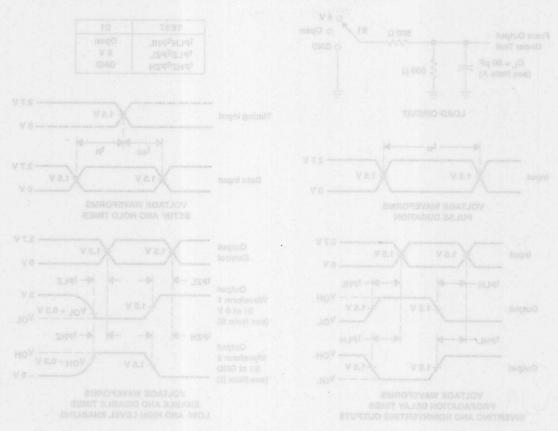
NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_r \leq 2.5 \, \text{ns}$, $t_f \leq 2.5 \, \text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C. Includes probe and its capacitant

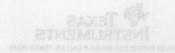
A Measurement of a to see collect with internal concilions such that the output when disabled by the output control.

Journal of the control of the contro

C. All Input guilses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZQ = 50 Q, ½ ≤ 2.5 ns, ½ ≤ 2.5 ns,

O: The culcula are measured one at a finite with one transition per measurement

Source 1. Load Circuit and Voltage Wavelorms



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 Members of the Texas Instruments Widebus™ Family 	SN54LVTH162245 WD PACKAGE SN74LVTH162245 DGG OR DL PACKAGE (TOP VIEW)
State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation	1DIR 1 48 1 0 1 0 181 2 47 1A1 1B2 3 46 1A2
A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required	GND 4 45 GND 1B3 5 44 1A3 1B4 6 43 1A4
High-Impedance State During Power Up and Power Down	V _{CC} 07 42 V _{CC} 185 08 41 1A5
Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})	1B6 9 40 1A6 GND 10 39 GND 1B7 11 38 1A7
Support Unregulated Battery Operation Down to 2.7 V	1B8 12 37 1A8 2B1 13 36 2A1
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	2B2 0 14 35 0 2A2 GND 0 15 34 0 GND 2B3 0 16 33 0 2A3
Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors	
Power Off Disables Outputs, Permitting Live Insertion	2B6 20 29 2A6 GND 21 28 GND
 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	2B7 0 22 27 0 2A7 2B8 0 23 26 0 2A8
Flow-Through Architecture Optimizes PCB Layout	2DIR (24 25) 2 OE

description

JESD 17

The 'LVTH162245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Widebus is a trademark of Texas Instruments Incorporated.



Latch-Up Performance Exceeds 500 mA Per

MIL-STD-883, Method 3015; Exceeds 200 V
Using Machine Model (C = 200 pF, R = 0)

Package Options Include Plastic 300-mil
Shrink Small-Outline (DL) and Thin Shrink
Small-Outline (DGG) Packages and 380-mil
Fine-Pitch Ceramic Flat (WD) Package
Using 25-mil Center-to-Center Spacings

ESD Protection Exceeds 2000 V Per

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description (continued)

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

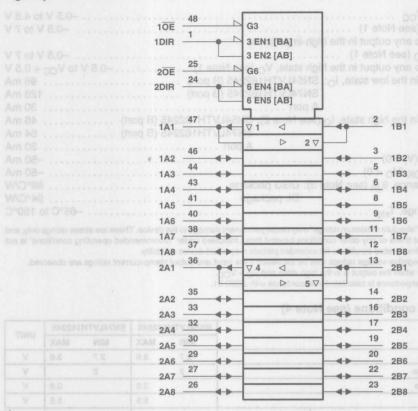
When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH162245 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74LVTH162245 is characterized for operation from -40° C to 85° C.

FUNCTION TABLE (each 8-bit section)

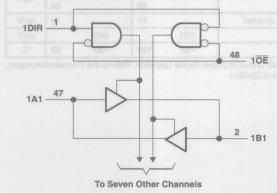
INP	UTS	ODEDATION
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

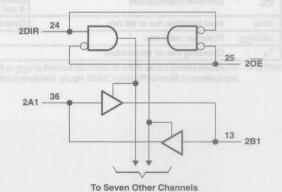
logic symbol treflic assimul appear crutaragmet ris-esti pritarago rovo agnitar mumixam etuloadi



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V	1
Input voltage range, V _I (see Note 1)	-0.5 V to 7 V	1
Voltage range applied to any output in the high-impeda		
		,
Voltage range applied to any output in the high state, V		
Current into any output in the low state, Io: SN54LVTH		
	H162245 (B port)	
	30 mA	
Current into any output in the high state, IO (see Note 2	2): SN54LVTH162245 (B port) 48 mA	1
	SN74LVTH162245 (B port) 64 mA	1
	A port	1
Input clamp current, I _{IK} (V _I < 0)		
Output clamp current, I _{OK} (V _O < 0)		
Package thermal impedance, θ _{JA} (see Note 3): DGG p		
	ckage 94°C/W	
Storage temperature range, T _{stq}	–65°C to 150°C	,
0.9		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

	385 - 45		SN54LVTH162245	SN74LVTH162245	
			MIN MAX	MIN MAX	UNIT
Vcc	Supply voltage		2.7 3.6	2.7 3.6	V
VIH	High-level input voltage	anno de marco de marco	2	2	V
VIL	Low-level input voltage		0.8	0.8	V
VI	Input voltage		5.5	5.5	٧
(min	on B17-12.	A port Old bris Mari	0 bis 39908M-12	sonshiocca ni e-12	NS ST
ЮН	High-level output current	B port	-24	-32	mA
l	Laurianal antonia annona	A port	(a) (a) (12)	vii(200) mm 12	- A
IOL	Low-level output current	B port	48	64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	10	10	ns/V
Δt/ΔVCC	Power-up ramp rate		200	200	μs/V
TA	Operating free-air temperature		-55 125	-40 85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS260J – JUNE 1993 – REVISED – MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	65	SSPINITYLINGS	BUSCLVENTS23A6	SN54LVT	H162245	SN74LVTH16	2245	
PAH	RAMETER	TEST C	ONDITIONS	MIN TY	PT MAX	MIN TYPT	MAX	UNIT
VIK		V _{CC} = 2.7 V,	I _I = -18 mA	175	-1.2	(dright)	-1.2	V
	JURISH PRINS	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0.2		Vcc-0.2		
	A port	V _{CC} = 3 V,	I _{OH} = -12 mA	2	B	2		rid.
	3.8	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0.2		V _{CC} -0.2		Hqt
VOH	8.4	V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	A	2.4		V
	B port	146 82	I _{OH} = -24 mA	2				Hat
301	5.6	V _{CC} = 3 V	I _{OH} = -32 mA		A 1	2		(24)
	8.8	V _{CC} = 2.7 V to 3.6 V,	I _{OL} = 100 μA		0.2		0.2	Zol
	A port	V _{CC} = 3 V,	I _{OL} = 12 mA		0.8		0.8	
	(8.6	0.71	I _{OL} = 100 μA		0.2		0.2	
v ===	5.5	V _{CC} = 2.7 V	I _{OL} = 24 mA		0.5	58	0.5	H97
VOL	8.4	1.6 3.5 6.1	I _{OL} = 16 mA		0.4		0.4	V
	B port	1.5 4 6.6	I _{OL} = 32 mA		0.5	55	0.5	
	8.8	VCC = 3 V	I _{OL} = 48 mA		0.55			
		a.0	I _{OL} = 64 mA				0.55	
	Control	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	1	= ±1	0.6 = 0.0 V fa one sau ±1.1		ingy! I
	inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	TOWN TOWN	10		10	
l _l			V _I = 5.5 V		20		20	μА
	A or B ports	V _{CC} = 3.6 V	$V_I = V_{CC}$		5		5	
			V _I = 0		-10	DISTRIBUTE.	-10	
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V		ASSESSMEN		±100	μΑ
len en	A or B ports	V 0.V	V _I = 0.8 V	75		75		
I(hold)	A or B ports	VCC = 3 V	V _I = 2 V	-75		-75		μА
lozpu		V _{CC} = 0 to 1.5 V, V _O = 0	0.5 V to 3 V, \overline{OE} = don't care		±100*		±100	μА
OZPD		V _{CC} = 1.5 V to 0, V _O = 0	0.5 V to 3 V, \overline{OE} = don't care		±100*		±100	μΑ
		V _{CC} = 3.6 V,	Outputs high		0.19		0.19	
lcc		I _O = 0,	Outputs low		5		5	mA
		V _I = V _{CC} or GND	Outputs disabled		0.19		0.19	
Δlcc [‡]	$V_{CC} = 3 \text{ V to } 3.6 \text{ V, One input at } V_{CC} - 0.6 \text{ V}$ Other inputs at V_{CC} or GND				0.3		0.2	mA
Ci		V _I = 3 V or 0			4	4		pF
Cio		V _O = 3 V or 0		THE THE	10	10		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

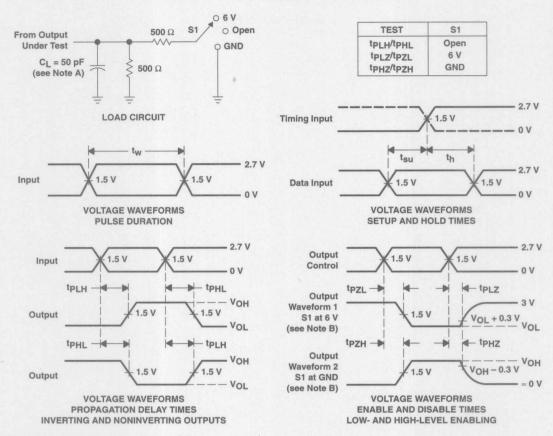
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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

22.43	SKYATALHIE	BACCOTHESER	s S	N54LVT	H162245	5		SN74	LVTH16	2245		man
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V	C = 3.3 ± 0.3 V	V	V _{CC} =	2.7 V	UNIT
	S.D-maV	5.0-	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
^t PLH	A	В	1	3.5	Am St.	4	1	2.3	3.3	7	3.7	ns
t _{PHL}	9.0-noV	S.O.	- 1	3.5	-100 uz	3.9	1	2.2	3.3	/	3.5	IIS
tPLH	В	A	1	4.3	Am 8-	5.3	1	2.8	4		4.6	ns
t _{PHL}	В	A	1	4.2	Am bis-	4.5	1	2.5	3.4		3.6	ns
^t PZH		В	1	4.8	Am SE-	5.9	1	2.8	4.6		5.4	
tPZL = 0	ŌĒ	D	1	4.8	An our	5.5	1	3	4.6		5.2	ns
tPZH = 0	ŌĒ	A	1	5.5	Act S7	7.2	1	3.3	5.3		6.3	
t _{PZL}	OE	8.0	1	5.4	Auxio:	6.4	1	3.3	5.1		5.8	ns
t _{PHZ}	ŌĒ	8.0 B	1.5	5.5	Am IS	5.8	1.5	3.8	5.2		5.5	
tPLZ	OE	B.0	1.5	5.5	Am 81	5.8	1.5	3.5	5.1		5.4	ns
tPHZ	ŌĒ	A	1.5	5.8	Arm SE	6.5	1.5	4	5.6		5.9	
tPLZ			1.2	6.3	· Am 81	6.3	1.5	3.8	5.5		5.5	ns
tsk(o) [‡]					Am.ba	e iol		NB T	0.5			ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ Skew between any two outputs of the same package switching in the same direction

PARAMETER MEASUREMENT INFORMATION

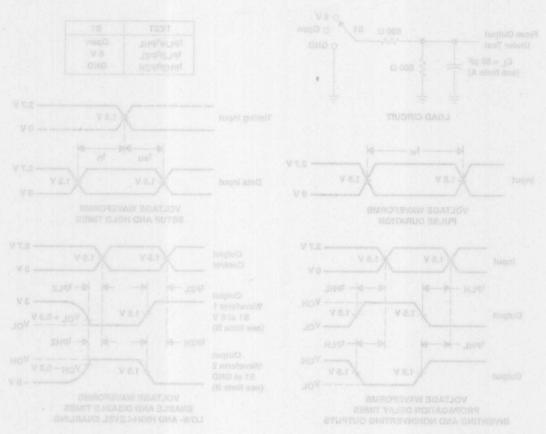


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- Annaliasana ni has adam aubulasi (C. A. 9777AV
- B. Waveform 1 is for an output with internal conditions such that the output low except when disabled by the output control.
- es, era e la reu era e la recue e O a reune os a usua recusarios esta Cumbrest aus Burabu suciente de Accondens ase besend indui ga "O
 - D. The outputs are measured one at a finte with one transition per measurement

Floure 1. Load Circuit and Voltage Waveforms



SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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•	Members of the Texas Instruments Widebus™ Family		SN54LVTH10 4LVTH16373				
evinb	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V		10E [BILL	VIEW)	1LE	
	Operation and Low Static Power Dissipation		1Q1		les .		
مالم			1Q2 L		ambed to E	1D2	
	Support Mixed-Mode Signal Operation		GND [and the second of the	GND	
	(5-V Input and Output Voltages With		1Q3 [1D3	
	3.3-V Vcc) a pigo bilav a ta afuqni atab pritsoft		1Q4 L	6	43	1D4	
	Support Unregulated Battery Operation		V _{CC}	7	42	VCC	
	Down to 2.7 V		1Q5 [8	41	1D5	
	High-Impedance State During Power Up		1Q6 [9	40	1D6	
	and Power Down		GND [E	GND	
	Typical V _{OLP} (Output Ground Bounce)		1Q7 [1000	A STATE OF THE PARTY OF THE PAR	1D7	
	< 0.8 V at V _{CC} = 3.3 V, T _A = 25°C		1Q8 [0.00		1D8	
	Bus Hold on Data Inputs Eliminates the		2Q1 [1,000		2D1	
	Need for External Pullup/Pulldown		2Q2 [0.00	E	2D2	
	Resistors		GND [P	GND	
			2Q3 [200		2D3	
	Power Off Disables Outputs, Permitting Live Insertion		2Q4 [47.47		2D4	
			V _{CC}			VCC	
•	Distributed V _{CC} and GND Pin Configuration		2Q5 [P	2D5	
	Minimizes High-Speed Switching Noise		2Q6 L		E	2D6	
•	Flow-Through Architecture Optimizes PCB		GND [GND	
	Layout		2Q7 [2270-0	E	2D7	
	Latch-Up Performance Exceeds 500 mA Per		2Q8 [200		2D8	
	JESD 17		20E [24	25	2LE	
•	ESD Protection Exceeds 2000 V Per						

description

The 'LVTH16373 devices are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

Widebus is a trademark of Texas Instruments Incorporated

MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings



SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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description (continued)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

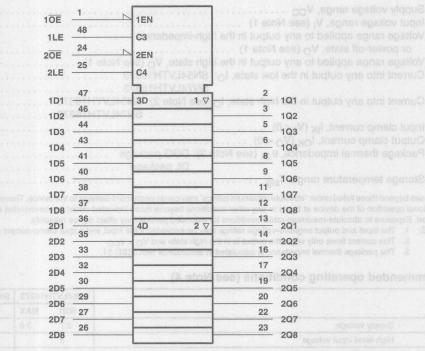
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

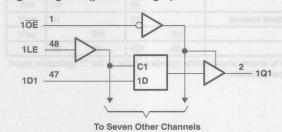
	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	olis Ligh
L	L	X	Q ₀
Н	X	X	Z

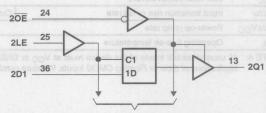
logic symbol the to acalmu) somer crusterequest via-east guitare or rovo agustar murrixam etvicada



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





To Seven Other Channels

SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Supply voltage range, VCC
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high-impedance
or power-off state, V _O (see Note 1)
Voltage range applied to any output in the high state, V _O (see Note 1)0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, Io: SN54LVTH16373
SN74LVTH16373
Current into any output in the high state, I _O (see Note 2): SN54LVTH16373 48 mA
SN74LVTH16373
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0)—50 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package
DL package
Storage temperature range, T _{stg}

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

	20		SN54LVT	H16373	SN74LVT	H16373	LINUT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	Control of the Contro	2.7	3.6	2.7	3.6	V
VIH	High-level input voltage	Annual statement and a state of	2		2		٧
VIL	Low-level input voltage	TER AND MINISTER AND LOS AND FOR	eus sanue	0.8	- contraction	0.8	V
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current		Yes	-24	Hanel I	-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔVCC	Power-up ramp rate		200	74	200		μs/V
TA	Operating free-air temperature	- B.15	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS SCBS144J - MAY 1992 - REVISED MARCH - 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	EZESTH	18373 SN74LV	SNS4LXTH	SN5	4LVTH16	373	SN74	4LVTH16	373	
PAI	RAMETER	TEST CONDIT	IONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	٧
	XAM MG3	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0	.2		VCC-0.	2		
art		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4			2.4	urabon, i	Puise d	
VOH		V - 0V	I _{OH} = -24 mA	2		I IB	esoted.	ine, dala	Setup ti	V
		VCC = 3 V	I _{OH} = -32 mA				2	na, dain	nif blaif	
		V 07V	I _{OL} = 100 μA			0.2			0.2	
		V _{CC} = 2.7 V	I _{OL} = 24 mA	denim	0001	0.5	oliene	dosta	0.5	
			I _{OL} = 16 mA	(1.0	HIBIAT.	0.4	paton	SPINA	0.4	Wiese V
VOL		V 0V	I _{OL} = 32 mA			0.5			0.5	V
		V _{CC} = 3 V	I _{OL} = 48 mA	Ven	01	0.55	MO	NR.	all the second	
		A (70.2	I _{OL} = 64 mA	L.J.	110431	10)	- EFUR	(P11)	0.55	
	KAM PINI	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	MILL		10			10	
. 970	Control inputs	V _{CC} = 3.6 V,	VI = VCC or GND	Marie Town	0	±1			±1	191
II SEE	4	V 00V	V _I = V _{CC}			1			1	μА
	Data inputs	V _{CC} = 3.6 V	V _I = 0		0	-5	-		-5	
loff	The same	V _{CC} = 0, V _I or V _O = 0 to 4.5	V						±100	μА
ha ha	Data inputs	V2-V	V _I = 0.8 V	75	0		75		D.	
II(hold)	Data inputs	VCC = 3 V	V _I = 2 V	-75			-75			μА
lozh	1.0	V _{CC} = 3.6 V,	V _O = 3 V	100000	0	5	37	5	5	μА
lozL	8.5	V _{CC} = 3.6 V,	V _O = 0.5 V			-5			-5	μΑ
lozpu		$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0.5$ V $OE = 0.5$ V	to 3 V,		0189	±100*	8.6 = mn	V Is one	±100	μА
lozpd		$\frac{V_{CC}}{OE}$ = 1.5 V to 0, V_{O} = 0.5 V OE	to 3 V,	eficilies of	podpeg a	±100*	to studie	o cari ya	±100	μА
			Outputs high			0.19		Espla	0.19	
Icc		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs low			5			5	mA
		Al = ACC of GIAD	Outputs disabled			0.19			0.19	
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input Other inputs at V _{CC} or GND	t at V _{CC} - 0.6 V,			0.2			0.2	mA
Ci		V _I = 3 V or 0			3			3		pF
Co		V _O = 3 V or 0			9			9		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

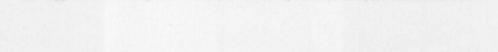
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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				5	SN54LV	ГН16373		5	SN74LV	ГН16373		ino
				V _{CC} = ± 0.	3.3 V 3 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high		2.4	3	- = HO	3		3	= sav-	3		ns
t _{su}	Setup time, data before	LE↓	9 1	2	-= 40	2		1		0.6		ns
th	Hold time, data after LE	L		3	-=40	3.3		1	- 00y	1.1		ns

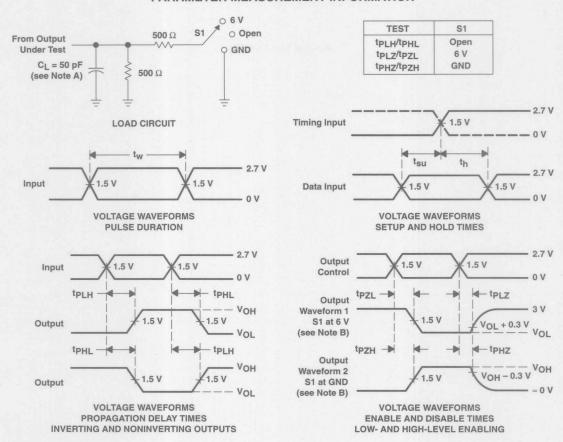
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

0.5		3.0	5	SN54LV	TH16373			SN74	LVTH16	6373	20
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	UNIT
(0)			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN MAX	
tPLH	D	Q	1.4	4.5	Vi w Vrse	5.2	1.5	2.7	3.8	4.2	
tPHL	D	Q	1.4	4.4	aV = IV	4.8	1.5	2.5	3.6	4	ns
tPLH	LE	0	1.8	5.5	0 = IV	5.8	2.1	3	4.3	4.8	
tPHL	LE	Q	1.8	5.2		5.6	2.1	2.9	4	4	ns
t _{PZH}	ŌĒ	0	1.4	5.7	8.0 ± 1V	6.7	1.5	2.8	4.3	5.1	
tPZL	OE		1.4	5.5	V S = iV	6	1.5	2.8	4.3	4.7	ns
tPHZ	ŌĒ	0	2	6	(Engl	6.2	2.4	3.5	5	5.4	ns
tPLZ	OE	4	1.4	5.2		5.6	2	3.2	4.7	4.8	115
tsk(o)‡		I was			3.48	o.s.V to	= ov v	0101.5	0.5		ns
All typical values a	are at V _{CC} = 3.3	3 V, T _A = 25°C.						anes l'inni	= 301		UNIX
		f the same package	switching	in the sa	ame direc	tion					



SCBS144J - MAY 1992 - REVISED MARCH - 1998

PARAMETER MEASUREMENT INFORMATION

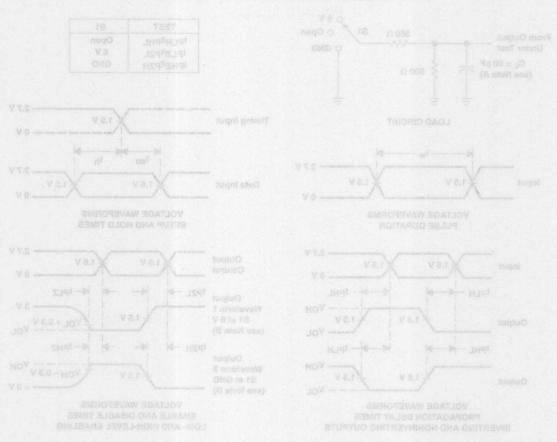


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Cuindudes probe and its repeatance
- Waveform 1 is for an output with informal conditions such that the output is low as: opi when disabled by the output confide.
 Waveform 1 is for an output with interest conditions such that output is high except when disabled by the output confide.
- All imput bulines are supplied by generators having the following characteristics: PHIS ± 10 MHz, ZQ = 50 Tz, Kr ± 2.5 ns, Q = 2.5 ns,
 - D. The outputs are measured one at a time with one trensmon per measurement.

Figure 1, Load Circuit and Voltage Waveforms



SN54LVTH162373, SN74LVTH162373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS2611 - JULY 1993 - REVISED MARCH 1998

•	Members of the Texas Instruments Widebus™ Family	SN54LVTH162373 D	GG OR DL PACKAGE
•	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power	10E 1	48 1 1LE 47 1 1D1
	Dissipation men a ferthe michaglic origin and easig of beau a	102 13	46 1D2
010	Output Ports Have Equivalent 22-Ω Series	GND 4	45 GND
	Resistors, So No External Resistors Are Required	1Q3 🛮 5 1Q4 🗓 6	44 1 1D3 43 1D4
elle	Support Mixed-Mode Signal Operation and bio stock of	lo enclived 7	42 VCC
	(5-V Input and Output Voltages With	1Q5 8	41 1 1D5
	3.3-V Voo)	1Q6 🛮 9	40 D 1D6
•	Support Unregulated Battery Operation	GND 10	39 GND
	Down to 2.7 V	1Q7 🛮 11	38 1D7
•	High-Impedance State During Power Up	1Q8 [12	37 D8
	and Power Down with a state of the state of	2Q1 13 0 n	36 2D1
	Typical V _{OLP} (Output Ground Bounce)	2Q2 14	35 2D2
	$< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$	GND 15	34 GND
00	Bus Hold on Data Inputs Eliminates the	2Q3 I 16	33 2D3
	Need for External Pullup/Pulldown	2Q4 17	32 2D4
	Resistors	V _{CC} 18	31 V _{CC}
	Power Off Disables Outputs, Permitting	2Q5 [19	30 2D5
	Live Insertion	2Q6 [] 20 GND [] 21	29 2D6 28 GND
	Distributed V _{CC} and GND Pin Configuration	2Q7 1 22	28 GND 27 2D7
	Minimizes High-Speed Switching Noise	2Q8 [23	26 2D8
•	Flow-Through Architecture Optimizes PCB Layout	2 0 E 24	25 2LE
•	Latch-Up Performance Exceeds 500 mA Per		

description

JESD 17

The 'LVTH162373 devices are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

Widebus is a trademark of Texas Instruments Incorporated.

ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings



SN54LVTH162373, SN74LVTH162373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS261I - JULY 1993 - REVISED MARCH 1998

description (continued)

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

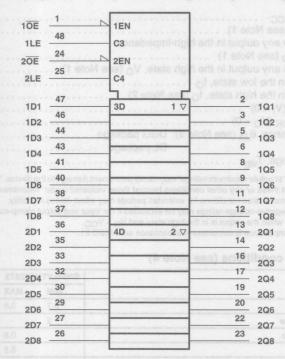
The SN54LVTH162373 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74LVTH162373 is characterized for operation from -40° C to 85° C.

FUNCTION TABLE (each 8-bit section)

	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	ROATSEZ
L	L	X	Q ₀
Н	X	X	Z

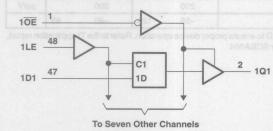


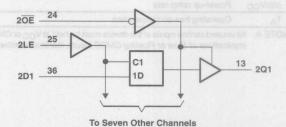
logic symbol tradio esetru) spraz erutaregnet ria-sert gnitarego revo agnitar munitare



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN54LVTH162373, SN74LVTH162373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, VO (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, IO	30 mA
Current into any output in the high state, IO (see Note 2)	30 mA
Input clamp current, I _{IK} (V _I < 0)	-50 mA
Output clamp current, IOK (VO < 0)	
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and VO > VCC.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

	204		SN54LVTH162373	SN74LVTH162373	UNIT	
			MIN MAX			
Vcc	Supply voltage		2.7 3.6	2.7 3.6	V	
VIH	High-level input voltage	Service Service Services Services	2	2	V	
VIL	Low-level input voltage		0.8	0.8	V	
VI	Input voltage	Section of the section of the section of	5.5	5.5	V	
ЮН	High-level output current	1 - 18 6/8 2331 NBM-12	sonsbroods ni s+12	mA		
loL	Low-level output current		12	12	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled	(sige10	vitigos) mm10	ns/V	
Δt/ΔVCC	Power-up ramp rate		200	200	μs/V	
TA	Operating free-air temperature	-55 125	-40 85	°C		

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54LVTH162373, SN74LVTH162373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS SCBS2611 – JULY 1993 – REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		SHZYCYTHIS	SN54	LVTH16	2373	SN74	LINUT			
		TEST C	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
VIK	00	V _{CC} = 2.7 V,	I _I = -18 mA		(TUPST)	-1.2	, FIU	38(1)	-1.2	٧
VOH	XAM HIM	V _{CC} = 3 V,	I _{OH} = -12 mA	2			2			V
VOL	1.8	V _{CC} = 3 V,	I _{OL} = 12 mA	BELL!	17	0.8	1		0.8	V
	B.本	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	91.0		10			10	497
l _l en	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	19.	- 6	±1			±1	
11	43-	V 00V	V _I = V _{CC}	18		1			1	μА
	Data inputs	V _{CC} = 3.6 V	V _I = 0	T L	73	-5	1	46	-5	
loff	18,8	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V	N. P.					±100	μА
1 201	A inputs	War OV	V _I = 0.8 V	75	1	- 1	75	× 111	2	
I(hold)		VCC = 3 V	V ₁ = 2 V	-75			-75			μА
lozh		V _{CC} = 3.6 V,	V _O = 3 V			5			5	μΑ
lozL		V _{CC} = 3.6 V,	V _O = 0.5 V		Q-765	-5	E = 01	V in enn	-5	μΑ
lozpu		$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$		Sit Holes d. II.	±100*	io anagi	on older de	±100	μΑ	
lozpo		$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = \frac{V_{CC}}{OE} = \frac{1.5 \text{ V to 0, V}_{O}}{OE} = 1.$	±100*			±100			μА	
			Outputs high	0.19		0.19		0.19		
lcc [‡]		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs low			5			5	mA
		AI - ACC OLGIAD	Outputs disabled			0.19	0.19			
		V _{CC} = 3 V to 3.6 V, On Other inputs at V _{CC} or	0.2			0.2			mA	
Ci		V _I = 3 V or 0	3			3			pF	
Co		V _O = 3 V or 0			9		9			pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN	SN54LVTH162373					SN74LVTH162373				
		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
t _W	Pulse duration, LE high	3		3		3		3		ns		
tsu	Setup time, data before LE↓	1.3		0.6		1		0.6		ns		
th	Hold time, data after LE↓	1		1.1		1		1.1		ns		

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH162373, SN74LVTH162373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS2611 - JULY 1993 - REVISED MARCH 1998

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

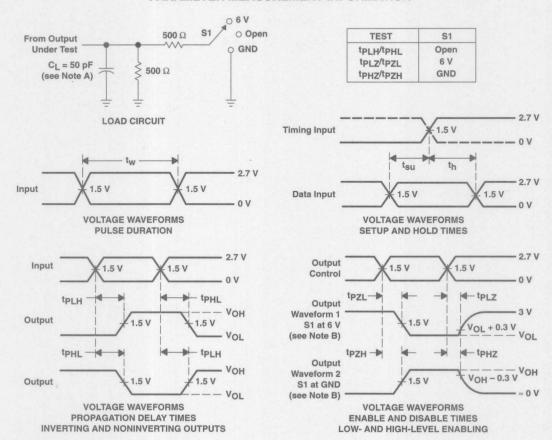
	SHAMMATALIE	BALLYTHI 62973	S	N54LVT	H16237	3		SN74	LVTH16	2373	-		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V		CC = 3.3 ± 0.3 V	V	V _{CC} =	2.7 V	UNIT	
	8		MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	Harry.	
tPLH 0	D	3 0 Q	1.8	5	-Am SI	5.7	1.9	3.1	4.6		5.1	ns	
tPHL	D		1.8	4.4	SV	4.8	1.9	2.8	4		4.3	IIS	
tPLH	1.5	Q	2.1	5.4	0.10	6.2	2.2	3.4	5.1	ehsten	5.8	200	
tPHL	LE	LE		2.1	4.9	00	4.7	2.2	3.2	4.6		4.3	ns
tPZH	ŌĒ	0	1.7	5.6		7	1.8	3.2	5.4	27(3)	6.6	200	
tPZL	OE	· ·	1.7	5.3	of 0 = 0	5.9	1.8	3.2	4.9		5.5	ns	
tPHZ	ŌĒ	Q	2.3	6.3	¥8	6.6	2.4	3.8	5.4		5.7		
tPLZ	OE		1	7.4	V	6.4	2.2	3.5	5.1		5	ns	
tsk(o)‡		10			V	=OV		Val	0.5			ns	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[†] Skew between any two outputs of the same package switching in the same direction

SCBS2611 - JULY 1993 - REVISED MARCH 1998

PARAMETER MEASUREMENT INFORMATION

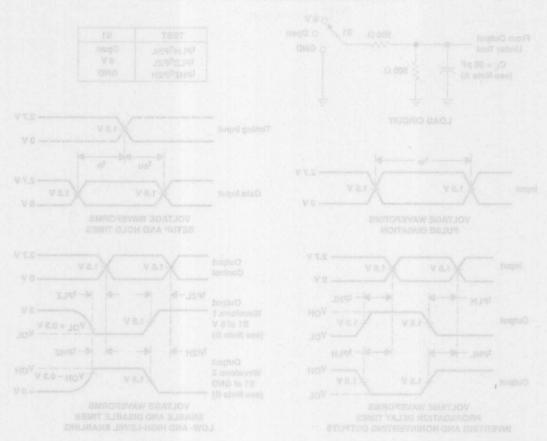


NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C. Includes probe and its dependance
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - free state and the contract one should be to the property and the other act. At

Figure 1, Load Circuit and Voltage Waveforms



SN54LVTH16374, SN74LVTH16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS145K - MAY 1992 - REVISED APRIL 1998

•	Members of the Texas Instruments <i>Widebus™</i> Family			1	WD PACKAGE DGG OR DL PACK VIEW)	
e vink	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V		10E		10LK	
	Operation and Low Static Power		1Q1	2	47 D1	
	Dissipation		102	3	46 1D2	
•	Support Mixed-Mode Signal Operation		GND	4	45 GND	
	(5-V Input and Output Voltages With		1Q3	5	44 1D3	
	3.3-V Vcc) at sign bilev at a study at a political to be	saunu t	1Q4	6	43 D4	
	Support Unregulated Battery Operation		Vcc	7	42 VCC	
	Down to 2.7 V		1Q5	8	41 1D5	
	High-Impedance State During Power Up		1Q6	9	40 1D6	
	and Power Down		GND	10	39 GND	
	Typical V _{OLP} (Output Ground Bounce)		107	1 1 2 1	38 1D7	
	< 0.8 V at V _{CC} = 3.3 V, T _A = 25°C		1Q8	4	37 D1D8	
	Bus Hold on Data Inputs Eliminates the AMAT HOL		2Q1		36 2D1	
	Need for External Pullup/Pulldown		2Q2		35 2D2	
			GND		34 GND	
	Power Off Disables Outputs, Permitting		2Q3		33 2D3	
	Live Insertion		2Q4	-	32 2D4	
			.00	18	31 V _{CC}	
	Distributed V _{CC} and GND Pin Configuration		2Q5	7	30 2D5	
	Minimizes High-Speed Switching Noise			20	29 2D6	
•	Flow-Through Architecture Optimizes PCB			21	28 GND	
	Layout		2Q7		27 2D7	
•	ESD Protection Exceeds 2000 V Per		2Q8	-	26 2D8	
	MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)		20E	24	25 2CLK	

description

JESD 17

The 'LVTH16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

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Latch-Up Performance Exceeds 500 mA Per

Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings



SCBS145K - MAY 1992 - REVISED APRIL 1998

description (continued)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

 $\overline{\text{OE}}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

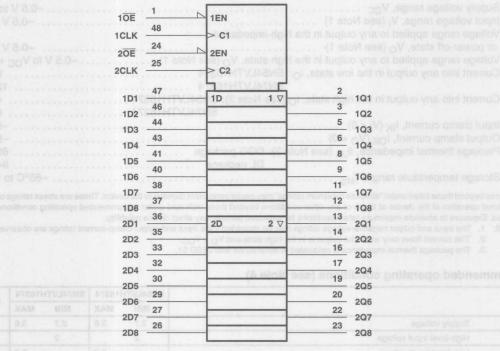
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE STATE AND ADDRESS OF THE STATE ADDRE

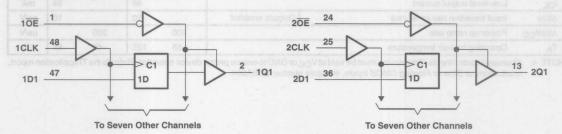
	INPUTS		OUTPUT
OE	CLK	D	Q
L	1	Н	Н
L	1	L	ohatugi
L	H or L	Х	Q ₀
Н	X	X	Z

logic symbol† ento assinu) egner erutaregnet ris-sert pottersoo revo agnitar municant



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCBS145K - MAY 1992 - REVISED APRIL 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V 0.5 V to 7 V
Voltage range applied to any output in the high-impedance	
or power-off state, VO (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Current into any output in the low state, IO: SN54LVTH16374	96 mA
SN74LVTH16374	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVTH16374	48 mA
SN74LVTH16374	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Package thermal impedance, θ _{IA} (see Note 3): DGG package	
DL package	94°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		Comment of the Comment of the State of the S	SN54LVTI	H16374	SN74LVT	H16374	1.15.117
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage	notanible Office ador.	o luo municio	0.8	-anniversa	0.8	V
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current		(4)	-24	(Elmons)	-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔVCC	Power-up ramp rate		200		200	5	μs/V
TA	Operating free-air temperature	- 3LIGG	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54LVTH16374, SN74LVTH16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS SCBS145K - MAY 1992 - REVISED APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TH16374	CIATUR	EXERTHTY IN EVER	SN54	LVTH16	374	SN74	LVTH16	374	LIMIT	
PAI	RAMETER	S.E w goV	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
VIK		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	٧	
	XAM VIIM	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0.	2		VCC-0.	.2			
xHM.		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4			2.4	yoneupe	Olgak Ir	Hook	
VOH		8	I _{OH} = -24 mA	2		W0110	rigid 2LJC	,notion,	Pulse d	V	
		VCC = 3 V	I _{OH} = -32 mA	wet to At	ollet	1711	2	me, date	g drises		
an	1.0	8.0	I _{OL} = 100 μA	woi to m	aH1	0.2	LIO refte	etab ,er	0.2		
		V _{CC} = 2.7 V	I _{OL} = 24 mA			0.5			0.5		
50 p		atulsteqmal tie-	I _{OL} = 16 mA	name of	10000	0.4	oldeine	el dens	0.4	vitchi	
VOL			I _{OL} = 32 mA	(1.6	ON PARTY	0.5	0.5		V		
	VCC = 3 V		I _{OL} = 48 mA			0.55					
		Vcc=33V	I _{OL} = 64 mA	Joy	03		. 180	A9	0.55		
		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	9	(1491)	10	(TU)	(1921)	10		
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	PM		±1			±1		
li _{selle}	081	- 081	V _I = V _{CC}	011		1			1×	μА	
	Data inputs	V _{CC} = 3.6 V	V ₁ = 0	H	- 0	-5	-5		-5		
loff	.4.2	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V						±100	μА	
-	5.4	1.5 2.8 4.5	V ₁ = 0.8 V	75	0		75		1	59	
II(hold)	Data inputs	V _{CC} = 3 V	V _I = 2 V	-75			-75			μΑ	
lozh	A.0	V _{CC} = 3.6 V,	V _O = 3 V	T III		5		5	5	μА	
OZL	8.8	V _{CC} = 3.6 V,	V _O = 0.5 V	NI DE		-5			-5	μА	
lozpu		V _C C = 0 to 1.5 V, V _O = OE = don't care	= 0.5 V to 3 V,		0.50	±100*	0.E = nc	V 16 808	±100	μА	
IOZPD		V _{CC} = 1.5 V to 0, V _O : OE = don't care	= 0.5 V to 3 V,	prietofikra by	peciong:	±100*	to enign	ny two ou	±100	μА	
			Outputs high			0.19			0.19		
lcc	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs low			5			5	mA	
		AI - ACC OL CHAD	Outputs disabled			0.19			0.19		
ΔICC [‡]		V _{CC} = 3 V to 3.6 V, Or Other inputs at V _{CC} or	ne input at V _{CC} – 0.6 V,			0.2			0.2	mA	
Ci		V _I = 3 V or 0			3			3		pF	
Co		V _O = 3 V or 0			9			9		pF	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LVTH16374			5	SN74LV1	TH16374		UNIT	
				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 ± 0.3 V		V _{CC} = 2.7 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		5.0		160	= uol	160	27V.	160		160	MHz
t _W	Pulse duration, CLK high	h or low	9 1	3	Am J.S.	3		3		3		ns
t _{su}	Setup time, data before	CLK1	High or low	2.9	Am SE-	3.3		1.8	:00A	2		ns
th	Hold time, data after CLI	K↑	High or low	0.8	Au do?	0.2		0.8		0.1		ns

switching characteristics over recommended operating free-air temperature range, C₁ = 50 pF (unless otherwise noted) (see Figure 1)

		188.0	SN54LVTH16374					SN74	LVTH16	6374		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
Ph.			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
f _{max}		1	160		160	V=WI	160			160		MHz
tpLH	CLK	Q	1.4	5.6		6.2	1.9	3	4.5	sindu	5.2	ns
tPHL	CLK	Q	1.7	4.8	0.0	5	2.1	2.9	4		4.2	113
^t PZH	ŌĒ	Q	1	5.6	VB	6.4	1.5	2.8	4.5		5.4	no
tpzL	OE	Q	1.4	5.5	V	6.2	1.5	2.8	4.4	ahign	5	ns
tPHZ	ŌĒ	Q	1	6.4	Vi	6.9	2.4	3.5	5		5.4	ns
tPLZ	OE	UE Q	1.7	5	15 X	5.2	2	3.2	4.6		4.8	115
t _{sk(o)} ‡					Vε	0.5 V to	DV.V	8.1 of 0 :	0.5			ns

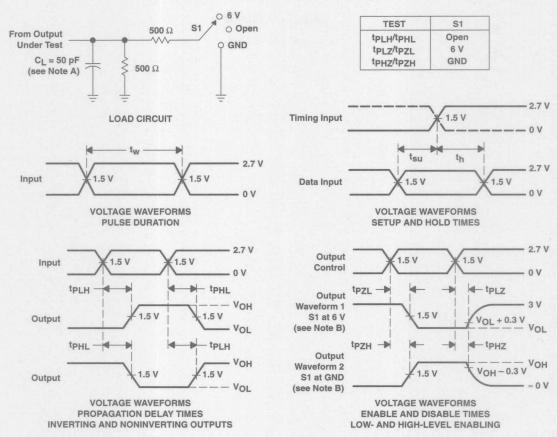
† All typical values are at VCC = 3.3 V, TA = 25°C.



All typical values are at $V_{CC}=3.3$ V, $T_A=25^{\circ}C$. Skew between any two outputs of the same package switching in the same direction

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PARAMETER MEASUREMENT INFORMATION

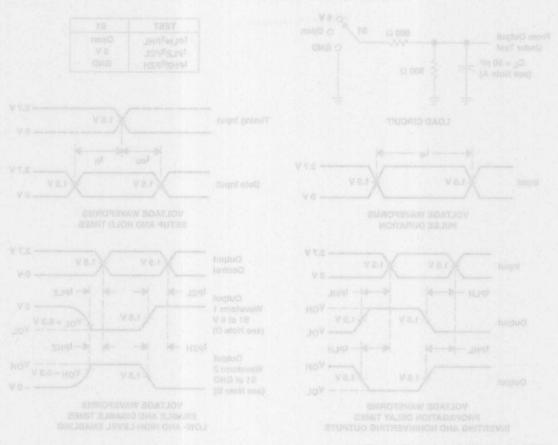


NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



VOTES: A. C. includes probe and ilg capacitance.

B. Waystorm 1 is for an output with internal conditions such that the output is low except when deathed by the output control.

Waystorm 2 is for an output with internal conditions such that the output is high except when deathed by the output control.

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Figure 1. Load Circuit and Voltage Waveforms



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•	Members of the Texas Instruments Widebus™ Family	SN54LVTH162374 WD PACKA SN74LVTH162374 DGG OR DL PA (TOP VIEW)	Section of the section of
(high drive	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation	1 OE 1 48 1CLK 1Q1 2 47 1D1 1Q2 3 46 1D2	
alid e	Output Ports Have Equivalent 22- Ω Series Resistors, So No External Resistors Are Required	GND 4 45 GND 1Q3 5 44 1D3 1Q4 6 43 1D4	
ot end	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})	V _{CC} 07 42 V _{CC} 1Q5 08 41 1D5 1Q6 09 40 1D6	
•	Support Unregulated Battery Operation Down to 2.7 V	GND 10 39 GND	
loen. Istor;	High-Impedance State During Power Up and Power Down	1Q8 12 37 1D8 2Q1 13 36 2D1	
• 25°C.	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C	2Q2 14 35 2D2 GND 15 34 GND 2Q3 16 33 2D3	
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors	2Q4 17 32 2D4 V _{CC} 18 31 V _{CC} 2Q5 19 30 2D5	
•	Power Off Disables Outputs, Permitting Live Insertion	GND 21 28 GND	
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise	2Q7 U 22 27 U 2D7 2Q8 U 23 26 U 2D8	
•	Flow-Through Architecture Optimizes PCB Layout		
•	Latch-Up Performance Exceeds 500 mA Per JESD 17		
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V		

description

The 'LVTH162374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

Widebus is a trademark of Texas Instruments Incorporated.

Using Machine Model (C = 200 pF, R = 0)
Package Options Include Plastic 300-mil
Shrink Small-Outline (DL) and Thin Shrink
Small-Outline (DGG) Packages and 380-mil
Fine-Pitch Ceramic Flat (WD) Package
Using 25-mil Center-to-Center Spacings



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description (continued)

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH162374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH162374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each flip-flop)

IN	IPUTS		OUTPUT
	CLK	D	Q
	1	Н	Н
	1	L	L
ŀ	HorL	X	Qo
	X	X	Z



To Seven Other Channels

logic symbol terto seeinu) egnet sture temperature transperature transperature sturies of the seeing symbol transperature transp 1EN 10E 48 1CLK 24 20E 2EN 25 2CLK > C2 47 1D1 1 7 Input clamp current, inc (VIQI) 1D 46 3 102 1D2 44 5 1Q3 1D3 43 6 1D4 1Q4 41 8 1D5 1Q5 40 9 1D6 1Q6 38 11 1D7 107 37 12 1D8 1Q8 36 13 2D1 2D 201 2 7 14 35 2D2 2Q2 33 16 2D3 2Q3 17 32 2D4 2Q4 19 30 2D5 2Q5 29 20 2D6 2Q6 27 22 2D7 26 23 2D8 2Q8 † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. logic diagram (positive logic) 10E 1 24 20E -25 1CLK -2CLK -> C1 > C1 13 2Q1 47 36 1D1 -1D 2D1 1D

To Seven Other Channels

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, IO	30 mA
Current into any output in the high state, Io (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, IOK (VO < 0)	
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DL package	
Storage temperature range, Teta	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVTH162374	SN74LVTH1	62374	
			MIN MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7 3.6	2.7	3.6	٧
VIH	High-level input voltage		2	2		V
VIL	Low-level input voltage	- Contracting the contraction	0.8		0.8	٧
VI	Input voltage	h	5.5		5.5	V
IOH	High-level output current	DATE controlled Dilling 199	-12	anacherena a	-12	mA
loL	Low-level output current		12		12	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	10	willabert m	10	ns/V
Δt/ΔVCC	Power-up ramp rate		200	200		μs/V
TA	Operating free-air temperature	-55 125	-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	374	SenityJatine	AVIOLETICALIS	SHOWLYT	SN54	LVTH16	2374	SN74LVTH16	2374	UNIT
PAI	RAMETER	VE 6 9 00V	CONDITIONS		MIN	TYPT	MAX	MIN TYPT	MAX	UNIT
VIK	1	V _{CC} = 2.7 V,	$I_{ } = -18 \text{ mA}$	V 5.0		(1031)	-1.2	(172(191))	-1.2	V
Vон	XAM NIM	V _{CC} = 3 V,	I _{OH} = -12 mA	XAM 9	2			2		V
VOL	Dar	V _{CC} = 3 V,	I _{OL} = 12 mA	1	11		0.8		0.8	V
80	2.8	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	8.8 4		0	10	20.00	10	Jel _
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND		±1			±1.	igi.	
li en-	8.8	8.8 8.8	V _I = V _{CC}	8.6		- 0	1	98	1	μА
	Data inputs	VCC = 3.6 V	V ₁ = 0	i a i	3		-5		-5	
loff	5.7.1	V _{CC} = 0,	V_I or $V_O = 0$ to	0 4.5 V		-		100	±100	μΑ
1.0.	Data insuta	8 8 S	V _I = 0.8 V	18 8	75			75		191
I(hold)	Data inputs	VCC = 3 V	V _I = 2 V -75 -75		10	μА				
lozh		V _{CC} = 3.6 V,	V _O = 3 V		MATE.	25°C.	5	are at Voc = 3.3		μΑ
lozL		V _{CC} = 3.6 V,	V _O = 0.5 V	ne ero ne on	(TOTAL B	DENDER G	-5	io embrano ovii vi	-5	μА
lozpu		$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	0.5 V to 3 V,				±100*		±100	μА
IOZPD		$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = \frac{V_{CC}}{OE} = \text{don't care}$	O = 0.5 V to 3 V,		±100*			±100		μА
			Outputs high				0.19		0.19	
loc		$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low				- 5		5	mA
		AL = ACC OL CLAD	Outputs disab	led	0.19		0.19	0.19		
∆lcc‡		V _{CC} = 3 V to 3.6 V, On Other inputs at V _{CC} or).6 V,			0.2		0.2	mA
Ci		V _I = 3 V or 0	100000000000000000000000000000000000000			3		3		pF
Co	PLEASE FOR DE	V _O = 3 V or 0				9		9		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			S	N54LVT	H162374	S	N74LVT	H162374			
			V _{CC} = ± 0.	± 0.3 V		V _{CC} = 2.7 V		3.3 V 3 V	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			160		160		160		160	MHz
t _W	Pulse duration, CLK high or low		3		3.3		3		3		ns
t _{su}	Setup time, data before CLK↑	High or low	2.8	- 3	3.2		1.8		2		ns
th	Hold time, data after CLK↑	High or low	1.2		0.5		0.8		0.1		ns

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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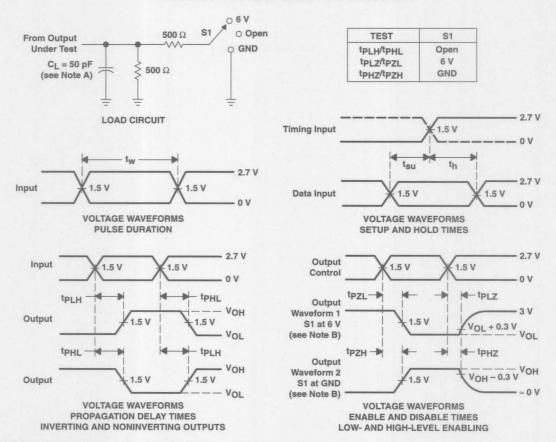
switching characteristics over recommended operating free-air temperature range, C1 = 50 pF (unless otherwise noted) (see Figure 1)

	SHYALVTHIS	IS 9LVTH162374	SN54LVTH162374			SN74LVTH162374					100		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT	
	8	9	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	1901	
fmax		1 8.0	160		160	= 101	160	V	=aaV	160		MHz	
tPLH	CLK	0	1.4	6.6	V a	7.4	2	3.4	5.3		6.2		
tPHL	CLK		1.4	5.8	D 10 00	6	2.2	3.3	4.9	atugni	5.1	5.1 ns	
tPZH	ŌĒ	Q	1	6.6	30	7.4	1.8	3.5	5.6		6.9	200	
tPZL	OE	Q .	1.4	6		6.8	1.8	3.5	4.9	BILIE	6	ns	
tPHZ	ŌĒ	Q	1	6.6	of 0 = a\	7.4	2.4	4.2	5.4		5.7		
tPLZ	OE		1.4	6	V a	6	2	3.8	5		5.1	ns	
tsk(o)‡	-75	i a			V	S=IV		V.S	0.5	SING	di Bizu	ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ Skew between any two outputs of the same package switching in the same direction

CBS262H - JULY 1993 - REVISED APRIL 1998

PARAMETER MEASUREMENT INFORMATION

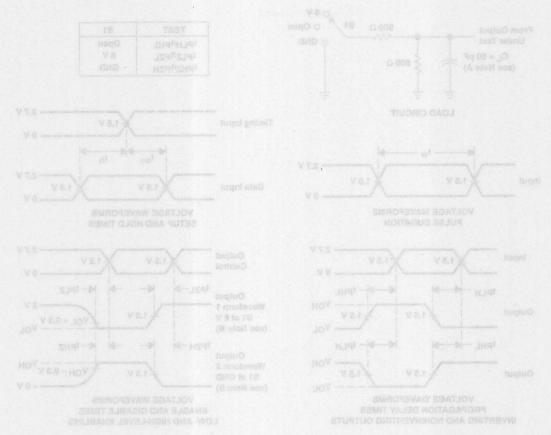


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,ns$, $t_f \leq 2.5 \,ns$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C. Includes probe and its depositance.
- Waveform 1 is for as output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an obtain after internal conditions such that the output is high accept when disabled by the output control.
- C. All input pulsos are exposed by generalists fronting the followers characteristics. PRR s 10 MHz. Zn = 60 tb t, < 2.5 ms. to 2.5 ms.
 - D. The outputs are measured one at a time with one transition per mappurement

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SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS701B - JULY 1997 - REVISED MARCH 1998

•	Members of the Texas Instruments Widebus™ Family	SN		0 0	WD PACKAGE DGG OR DL PACKAGE VIEW)
•	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation		OEAB [LEAB [A1 [1	56 GND 55 CLKAB 54 B1
no Bis	UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode		A2 [A3 [4 5 6 7	53 GND 52 B2 51 B3 50 VCC
•	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})		A5 [8	49 B4 48 B5
•	Support Unregulated Battery Operation Down to 2.7 V		GND [10 11	47 B6 46 GND
•	High-Impedance State During Power Up and Power Down		A8 [12 13 14	45 B7 44 B8
•	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C		A10 [14 15 16	43 B9 42 B10 41 B11
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors		A12 [GND [17 18 19	40 B12 39 GND 38 B13
•	Power Off Disables Outputs, Permitting Live Insertion			20	37 B14 36 B15
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise		A16 [22 23	35 V _{CC} 34 B16
•	Flow-Through Architecture Optimizes PCB Layout		GND [24 25	33 B17 32 GND
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package		OEBA [26 27 28	31 B18 30 CLKBA 29 GND

description

The 'LVTH16500 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (\overline{CLKAB} and \overline{CLKBA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CLKAB} is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of \overline{CLKAB} . Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

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SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS701B - JULY 1997 - REVISED MARCH 1998

description (continued)

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54LVTH16500 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16500 is characterized for operation from –40°C to 85°C.

FUNCTION TABLET

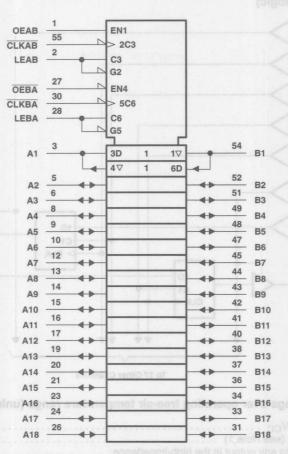
	INP	UTS		OUTPUT
OEAB	LEAB	CLKAB	Α	В
L	Х	X	X	Z
АН	Н	X	L	d Byuno
A H	Н	X	Н	H
AH	L	1	LB	ningtes f
H	L	1	Н	H
AH	L	Н	X	B ₀ ‡
Н	L	L	X	B ₀ ‡

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low





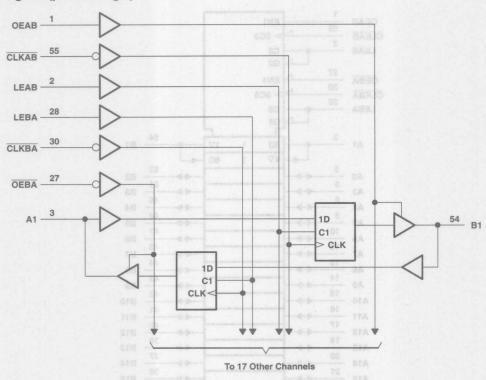
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high-impedance
Voltage range applied to any output in the high-impedance or power-off state, V _O (see Note 1)
Voltage range applied to any output in the high state, Vo (see Note 1)0.5 V to Vcc + 0.5 V
Current into any output in the low state, IO: SN54LVTH16500
SN74LVTH16500
Current into any output in the high state, IO (see Note 2): SN54LVTH16500
SN74LVTH16500
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0)
Package thermal impedance, θ, IA (see Note 3): DGG package
DL package
Storage temperature range, T _{stg} 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

^{3.} The package thermal impedance is calculated in accordance with JESD 51.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This current flows only when the output is in the high state and $V_O > V_{CC}$.

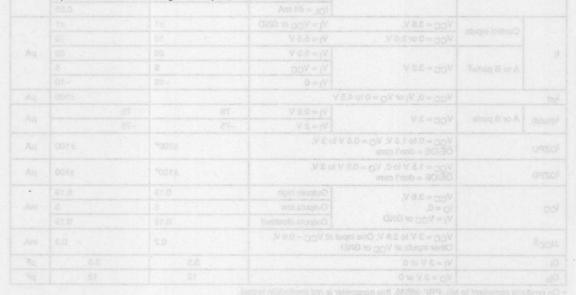
SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS701B - JULY 1997 - REVISED MARCH 1998

recommended operating conditions (see Note 4)

			SN54LVT	H16500	SN74LVTI	H16500	UNIT
		MIN	MAX	MIN	MAX	AG	
Vcc	Supply voltage	en gjellege kriste gjellege en kriste et kriste kriste (oktober	2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage	Amalesi	2	1.5 = 00	2		V
VIL	Low-level input voltage	AU DOI HO	A Bre of A	0.8	Y.	0.8	٧
VI	Input voltage	Am #= = HO		5.5	Y.	5.5	V
ЮН	High-level output current	Am AS- = HG!		-24	V	-32	mA
loL	Low-level output current	Ant Se- • HO!		48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	V	10	V	10	ns/V
Δt/ΔVCC	Power-up ramp rate	ART PE = JOY	200		200		μs/V
TA	Operating free-air temperature	Vill of a 1011	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.





SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS701B – JULY 1997 – REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DA	- 444ETED 1911	TEST COM	DITIONS	SN54LVTH16	6500	SN74	LVTH16	5500	UNIT
PAI	RAMETER	TEST CON	DITIONS	MIN TYPT	MAX	MIN	TYPT	MAX	UNI
VIK	e	V _{CC} = 2.7 V,	I _I = -18 mA		-1.2	erloy too	ni biscul-r	-1.2	٧
V	8.0	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.2		VCC-0.	2	den l	
		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4		2.4	snatlov t	estri .	V
VOH		V 48 0 V	I _{OH} = -24 mA	2	Inc	ences beauti	io lauralie	foilet	V
		V _{CC} = 3 V	I _{OH} = -32 mA		In	2	un Iniumb	sin I	
Vien	10	V-1 07V	I _{OL} = 100 μA		0.2	o a sis po	llied out b	0.2	19.50
		V _{CC} = 2.7 V	I _{OL} = 24 mA	The state of the same	0.5	elet om	m nu-re	0.5	way o
		1881 88-	I _{OL} = 16 mA		0.4	mat viscos	ed antho	0.4	V
VOL		and the second second second second	I _{OL} = 32 mA	I false for the ten and	0.5	a handile	advino be	0.5	V
		V _{CC} = 3 V	I _{OL} = 48 mA	MOS Inputs, litera	0.55	Implications of Slow or F			
			I _{OL} = 64 mA	pL = 64 mA				0.55	
	Control in mate	V _{CC} = 3.6 V,	V _I = V _{CC} or GND		±1		-14-	±1	
Control inputs		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V		10			10	
lį		出现家里于 为可能的	V _I = 5.5 V		20			20	μА
	A or B ports‡	V _{CC} = 3.6 V	V _I = V _{CC}		5		5		
		DECEMBER 18	V _I = 0		-10	-10		-10	
loff		V _{CC} = 0, V _I or V _O = 0 to 4	1.5 V					±100	μΑ
	A as D ands	V 0.V	V _I = 0.8 V	75		75			A
I(hold)	A or B ports	VCC = 3 V	V _I = 2 V	-75	-75			μА	
lozpu		$\frac{V_{CC}}{OE/OE} = 0 \text{ to } 1.5 \text{ V, } V_{O} = 0.5$	5 V to 3 V,	±100*		±100		±100	μА
lozpd		$\frac{V_{CC}}{OE/OE} = 1.5 \text{ V to 0, V}_{O} = 0.8$	5 V to 3 V,	±100*		±100		μА	
		V _{CC} = 3.6 V,	Outputs high		0.19			0.19	
Icc I		$I_{O} = 0$,	Outputs low		5			5	m/
		V _I = V _{CC} or GND	Outputs disabled	0.19		0.19			
ΔI _{CC} § V _{CC} = 3 V to 3.6 V, One input Other inputs at V _{CC} or GND				0.2			0.2	m/	
Ci		V _I = 3 V or 0		3.5			3.5		pF
Cio		V _O = 3 V or 0		12			12		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ Unused pins at V_{CC} or GND

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	rest		5	SN54LV	TH16500	100		SN74LV	TH16500			
				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		3.3 V 3 V	Vcc=	2.7 V	UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	0	
f _{clock} Clock frequence	;y			150		125		150		125	MHz	
. Data danta	LE high	TELEVISION I	3.3		3.3	127	3.3	-	3.3			
t _W Pulse duration	CLK high or low	-	3.3		3.3		3.3		3.3		ns	
11.0	A before CLKAB↓		1.8		1.1		1.8	O UNU	1.1			
	B before CLKBA↓	B before CLKBA↓			1.2		1.9		1.2			
t _{SU} Setup time	77 207 7	CLK high	2.2		1.3		2.2	wi	1.3	PERM	ns	
	A or B before LE↓	CLK low	2.7	8.712	1.9		2.7		1.9			
Varix	A or B after CLK↓	bigni e	1.2		1.2	V are	1.2		1.2		mogni	
th Hold time	ne A or B after LE↓		0.9	6.0	1.1	or other teams	0.9		1.1	-20,000	ns	

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

K	V 1.5 V 1.5 V		Tadano 6	SN54LVTH16500				SN74	LVTH16	5500	201015	13
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
fmax	1.sv T. Val	K. Isaaci	150		125	Va	150	N.B.	N	125	had	MHz
tPLH	B or A	A or B	1.7	5.8	JC	7	1.7	3	5.4		6.8	
tPHL SMS		BorA	AOIB	1.6	6		7.8	1.6	3.2	5.9	N-air	7.7
tPLH	LEDA LEAD	A or B	2.3	7.3	100	8.9	2.3	4	7		8.5	ns
t _{PHL}	LEBA or LEAB	BA OF LEAD A OF B	2.7	8.2		9.8	2.7	4.3	7.9		9.7	113
tPLH	CLKBA or	A or B	2	7.4		8.8	2	4.1	7		8.3	
^t PHL	CLKAB	AUIB	2.4	8.1		10	2.4	4.4	7.9	MON	9.9	ns
^t PZH	OFPA - OFAP	A or B	1.2	5.2		6.1	1.2	3	5	WAOHAI	5.9	200
tPZL	OEBA or OEAB	AOIB	1.5	5.9		7	1.5	3	5.8	the states	6.9	ns
tPHZ	OFFIA OFAF	A or B	2.7	7.7		8.6	2.7	4.6	7.4	embiden	8.3	REST
tPLZ	OEBA or OEAB	AUID	2.8	7.3	ALL STREET	7.7	2.8	4.7	6.7	T MINO BY	7.2	ns
tsk(o)‡	24 D08=DX 54	MOF≥RMS recit	naracted	o onlyod	of est on	vait evol	neneg ş	d beimgi	0.5	eluq fuqi	illA ,O	ns

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

‡ Skew between any two outputs of the same package switching in the same direction

PARAMETER MEASUREMENT INFORMATION 0 6 V TEST S1 500 Ω S1 O Open From Output Open tPHL/tPLH **Under Test** O GND tpLZ/tpZL 6 V CL = 50 pF tPHZ/tPZH GND 500 Ω (see Note A) 1.5 V LOAD CIRCUIT **Timing Input** th tsu 2.7 V Input 1.5 V 1.5 V 1.5 V 1.5 V **Data Input** 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V 1.5 V 1.5 V Input Control 0 V 0 V **tPLH tPHL** - tpLZ Output VOH Waveform 1 1.5 V 1.5 V 1.5 V S1 at 6 V Output VOL + 0.3 V VOL VOL (see Note B) - tPHZ **tPLH** tPZH → tPHL -Output VOH VOH Waveform 2 VOH - 0.3 V 1.5 V 1.5 V 1.5 V Output S1 at GND - VOL ≈ 0 V (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES** INVERTING AND NONINVERTING OUTPUTS LOW- AND HIGH-LEVEL ENABLING

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_0 = 50 Ω , $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS700B - JULY 1997 - REVISED MARCH 1998

•	Members of the Texas Instruments Widebus™ Family	SN7	4LVTH16501	I [WD PACKAGE	AGE
	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation		OEAB [LEAB [A1 [2	56 GND 55 CLKAB 54 B1	
o di	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})		GND [A2 [10000	53 GND 52 B2	
•	Support Unregulated Battery Operation Down to 2.7 V		V _{CC}	7	51 B3 50 V _{CC}	
•	High-Impedance State During Power Up and Power Down		A4 [A5 [9	49 B4 48 B5	
•	UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode		A6 [GND [A7 [A8 [A9 [11 12 13	47 B6 46 GND 45 B7 44 B8 43 B9	
•	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C		A10 [15	42 B10 41 B11	
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors		A12 [GND [A13 [17 18	40 B12 39 GND 38 B13	
•	Power Off Disables Outputs, Permitting Live Insertion		A14 [A15 [37 B14 36 B15	
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise		V _{CC} [23	35 V _{CC} 34 B16	
•	Flow-Through Architecture Optimizes PCB Layout		A17 [GND [25	33 B17 32 GND	
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package		OEBA [27	31 B18 30 CLKBA 29 GND	

description

The 'LVTH16501 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

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Using 25-mil Center-to-Center Spacings



SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS700B - JULY 1997 - REVISED MARCH 1998

description (continued)

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54LVTH16501 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16501 is characterized for operation from –40°C to 85°C.

FUNCTION TABLET

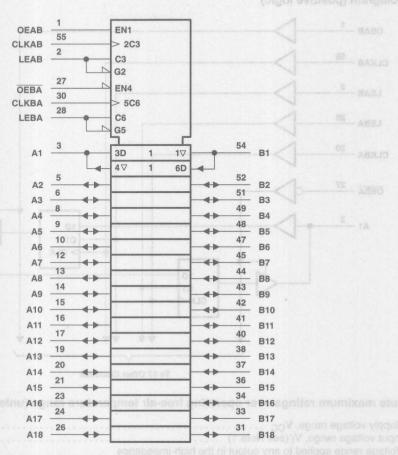
A	INPUTS						
OEAB	EAB LEAB CLK		A	В			
L	Х	X	X	Z			
AH	Н	X	L	somue s			
AH	Н	X	Н	H			
AH	L	1	L	ningtos f			
Н	L	1	Н	HOO			
AH	L	Н	X	B ₀ ‡			
Н	L	L	X	B ₀ §			

[†]A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

[§] Output level before the indicated steady-state input conditions were established





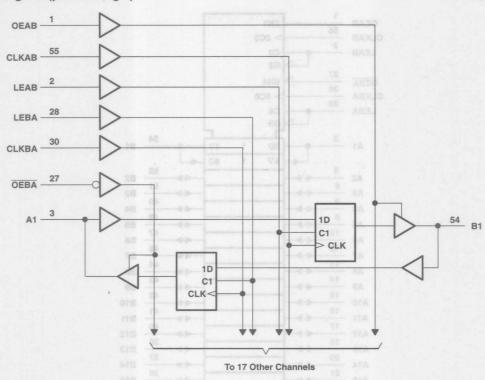
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS700B - JULY 1997 - REVISED MARCH 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	
Voltage range applied to any output in the high state, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, IO: SN54LVTH16501	96 mA
	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVTH16501	48 mA
SN74LVTH16501	64 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

^{3.} The package thermal impedance is calculated in accordance with JESD 51.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This current flows only when the output is in the high state and $V_O > V_{CC}$.

SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LVT	H16501	SN74LVT		
		SMOUTHOUSE	MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage	Americal	2	7.2 = 0.7	2		٧
VIL	Low-level input voltage	OA WILDOL = HOL	A GE OLA	0.8	X	0.8	V
VI V	Input voltage	Am 6-9 HO	- 8	5.5		5.5	V
ЮН	High-level output current	ART AST TO HOT		-24	W	-32	mA
loL	Low-level output current	S/II S(-= HO)		48	-	64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	V	10	V	10	ns/V
Δt/ΔVCC	Power-up ramp rate	F(II PS = 101	200		200		μs/V
TA	Operating free-air temperature	W01-01 a 701	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report,



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

1000	VAIN VIIM	TEST CON	DITIONS	SN54	LVTH16	6501	SN7	4LVTH16	5501	11011
PAI	RAMETER	TEST CON	DITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNI
VIK		V _{CC} = 2.7 V,	$I_{ } = -18 \text{ mA}$			-1.2	affine his	and leavest-	-1.2	V
V	8.0	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.	2	-	VCC-0	.2	wo.l	
V-V		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4			2.4	apatiou I	ironi	V
VOH		V _{CC} = 3 V	I _{OH} = -24 mA	2		lege	Dies Teath	un Inval	dolf-i	V
Am	48	ACC = 2 A	I _{OH} = -32 mA			in	2	un feval	Same A	
Vien	l or	V _{CC} = 2.7 V	I _{OL} = 100 μA			0.2	in make m	Minnset I	0.2	VE
		VCC = 2.7 V	I _{OL} = 24 mA			0.5	mien din	THE STATE	0.5	
		-55 128	I _{OL} = 16 mA			0.4	may vin-s	and condition	0.4	V
VOL			I _{OL} = 32 mA	history	ink resuped	0.5	s abinoi l	naturan he	0.5	V
	decompany of the Acc = 3 A to enter ledge		I _{OL} = 48 mA	noni stu	MOS Inc	0.55	P TO WO	IB to and	implicati	
			I _{OL} = 64 mA	-					0.55	
	0-1-1:1	V _{CC} = 3.6 V,	VI = VCC or GND			±1	-		±1	
Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10			10		
lį			V _I = 5.5 V		20				20	μА
A or B ports‡	V _{CC} = 3.6 V	V _I = V _{CC}			1	1				
			V ₁ = 0			-5	-5			
loff		VCC = 0, VI or VO = 0 to 4	.5 V						±100	μА
	A D d-	V 0V	V _I = 0.8 V	75	13.5	4	75			
I(hold)	A or B ports	VCC = 3 V	V _I = 2 V	-75			-75	The La		μА
lozpu		$\frac{V_{CC}}{OE/OE} = 0$ to 1.5 V, $V_{O} = 0.5$	5 V to 3 V,			±100*			±100	μА
IOZPD		$\frac{\text{V}_{\text{CC}} = 1.5 \text{ V to 0, V}_{\text{O}} = 0.5}{\text{OE}/\text{OE} = \text{don't care}}$	5 V to 3 V,			±100*			±100	μΑ
		V _{CC} = 3.6 V,	Outputs high			0.19			0.19	
Icc		I _O = 0,	Outputs low			5			5	m/
	V _I = V _{CC} or GND		Outputs disabled		0.19		C		0.19	
ΔICC§		V _{CC} = 3 V to 3.6 V, One in Other inputs at V _{CC} or GN				0.2			0.2	mA
Ci		V _I = 3 V or 0			3.5			3.5		pF
Cio		V _O = 3 V or 0			12	1102	100	12		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW

 $^{^{\}dagger}$ All typical values are at VCC = 3.3 V, TA = 25°C. ‡ Unused pins at VCC or GND

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS700B - JULY 1997 - REVISED MARCH 1998

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

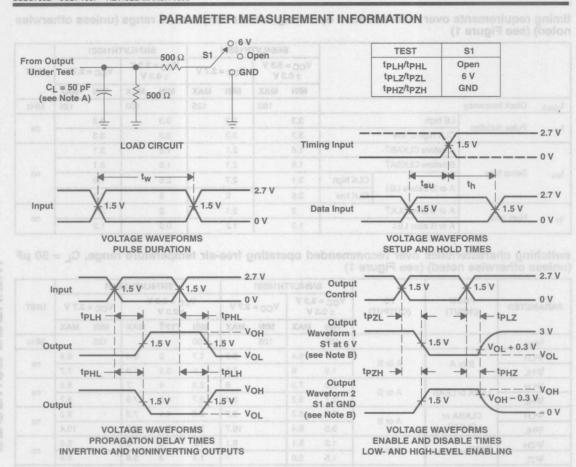
12	TEST		5	SN54LV1	TH16501	198	5	SN74LV	TH16501				
			V _{CC} =		V _{CC} =	2.7 V	V _{CC} = ± 0.		V _{CC} =	2.7 V	UNIT		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	(3)		
fclock Clock frequency			150		125		150		125	MHz			
t Dules direction	LE high		3.3		3.3		3.3	1	3.3		ns		
t _W Pulse duration	CLK high or low	rakeris.	3.3		3.3		3.3		3.3		115		
V 6	A before CLKAB↑	and and	1.6		2.1		1.6	O GAO.	2.1				
	B before CLKBA↑		1.6		2.1		1.6		2.1				
t _{su} Setup time		CLK high	3.1		2.7		2.6	(g)	1.9		ns		
	A or B before LE↓	CLK low	2.6	1111	2		2		1.3		1100		
t Halder	A or B after CLK↑		2		2.1	r air	2		2.1		undin		
th Hold time	A or B after LE↓	A or B after LE↓		A or B after LE↓ 1.3		V-0	1.2		0.9		1.2		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

	Val H	TO (OUTPUT)	Jugaro 6	SN54LV7	TH16501		V 8.7	SN74	LVTH16	6501	20000	
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V	CC = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
fmax	1.5.V		150		125	y e	150	V S	1	125	Tarrest	MHz
tPLH	D av A	A or B	1.7	5.4		6.8	1.7	3	5.4		6.8	ns
t _{PHL}	BorA	AOIB	1.6	6		7.8	1.6	3.2	5.9	Di- JRF	7.7	115
tPLH	LEBA or LEAB	A or B	2.3	7.3	330	9	2.3	4	7		8.5	ns
tPHL		AUIB	2.7	8.2		9.8	2.7	4.3	7.9		9.7	113
tPLH	CLKBA or	A or B	2.5	8.3	.30	9.7	2.5	4.1	7.9		9.2	200
tPHL	CLKAB	A or B	3.5	9.4		10.7	3.5	5.4	8.9	DOV	10.4	ns
^t PZH	OFFIA A OFAR	A or B	1.2	5.1		6.1	1.2	3	5	ASONS	5.9	
tPZL	OEBA or OEAB	AUID	1.5	5.9		7	1.5	3	5.8	OF SERVICE	6.9	ns
t _{PHZ}	OFFIA OF AR	A or B	2.7	7.5		8.5	2.7	4.6	7.4	sebuloni	8.3	-8310
tPLZ	OEBA or OEAB	B A or B	2.8	6.8	HOILS SILK	7.5	2.8	4.7	6.7	F FINGLEY	7.2	ns
tsk(o) [‡]	42.20=500,15	More BAB s 10 M	elescentri	o privide	of extrans	ved anot	y genera	d bullqqu	0.5	shiq fuqr	INA .S	ns

 † All typical values are at VCC = 3.3 V, TA = 25°C. ‡ Skew between any two outputs of the same package switching in the same direction





NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH16541, SN74LVTH16541 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS691C - MAY 1997 - REVISED APRIL 1998

•	Members of the Texas Instruments Widebus™ Family		SN741	LVTH1654	11	WD PAC DGG OR DL VIEW)	
•	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation			1 0E1 1Y1 1Y2	1 2	48 10 47 1A 46 1A	I and some
•	/E 1/ I 1 O -1 1 1/- II 1 1/III			GND	4 5	45 GN	The SNS4LQ
•	Support Unregulated Battery Operation Down to 2.7 V			V _{CC}		42 V _C	
•	High-Impedance State During Power Up and Power Down	A		1Y6 GND		40] 1A6 39] GN	
•	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C			1Y7 1Y8	12	38 1 1A	3
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors				14 15	36 2A 35 2A 34 GN	2 D
•	Power Off Disables Outputs, Permitting Live Insertion			2Y3 2Y4 V _{CC}	17	33 2A3 32 2A4 31 V _C	gic symbol [†]
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise	her		2Y5 2Y6	19	30 2AS	5
•	Flow-Through Architecture Optimizes PCB Layout			GND 2Y7	F101	28 GN 27 2A	7
•	Latch-Up Performance Exceeds 500 mA Per JESD 17	r		2Y8 2OE1		26 2A8 25 20	
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)				AT AT		
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings						

description

These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

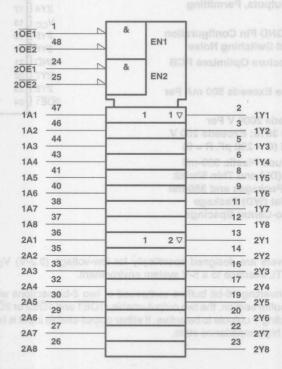
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH16541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

	INPUTS		OUTPUT
OE1	OE2	Α	Y
L	L	L	Loon
L	L	Н	Н
Н	X	X	Z
X	Н	X	Z

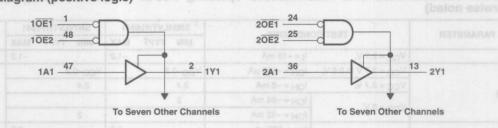
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	Am 8t = 101	
Input voltage range, V _I (see Note 1)	Am \$6 = 101	0.5 V to 7 V
Voltage range applied to any output in the hi		
or power-off state, VO (see Note 1)		
Voltage range applied to any output in the hi		
Current into any output in the low state, Io:	SN54LVTH16541	96 mA
		128 mA
Current into any output in the high state, IO	(see Note 2): SN54LVTH	16541 48 mA
	SN74LVTH	16541 64 mA
Input clamp current, I _{IK} (V _I < 0)	A 9% of B 44 OA 40 4A	–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Package thermal impedance, θ _{JA} (see Note	3): DGG package	89°C/W
Ai a	DL package	94°C/W
Storage temperature range, T _{stq}		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and VO > VCC.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

Am.	0.2	A 90 - 20A le 15dul	SN54LVT	H16541	SN74LVT	LINUT	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage						V
VIL	Low-level input voltage	range included on all steel	OFFICE A	0.8	ment to min	0.8	٧
VI	Input voltage	Input voltage 100 000 medicantal lavel agatev 113 ballsage and to a tall s				5.5	V
ЮН	High-level output current		A	-24		-32	mA
loL	Low-level output current		3	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	0	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate		200		200		μs/V
TA	Operating free-air temperature	-55	125	-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		1	OUDITIONS	SN54	LVTH1	6541	SN7	4LVTH16	541	
PAF	RAMETER	TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNI
VIK	MINE HIM SE	V _{CC} = 2.7 V,	I _I = -18 mA		*	-1.2			-1.2	V
	IV9	V _{CC} = 2.7 V to 3.6 V,	IOH = -100 μA	VCC-0.	2		VCC-0	.2		
.,		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4			2.4			V
VOH		V 0.V	I _{OH} = -24 mA	2	7					V
		VCC = 3 V	I _{OH} = -32 mA	or Chalille	wall no	ve8 of	2			
		V 07V	I _{OL} = 100 μA			0.2			0.2	
		V _{CC} = 2.7 V	I _{OL} = 24 mA	Mines	ado re	0.5	nilet.	Mum	0.5	mig
Vol. of V a 0-			I _{OL} = 16 mA			0.4	/ anno	n ensil	0.4	Lev
		Waa a 2 W	I _{OL} = 32 mA		(t at	0.5	W.ep	0.5		
		VCC = 3 V	I _{OL} = 48 mA	ort ent n	i juqiu	0.55	of beliggs egnal ear			loV
			I _{OL} = 64 mA		of edu	ow No	oV is	ters tho-	0.55	10
+ 0.5	OBV of V 8.0-	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	gri, edit d	Disdiri	\$ 10	il beliq	ga egni	10	OA
m 88	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	G (0) '81	PAS AN	±1	IHQIUO	VNB O	±1	UO.,
128 m		V _{CC} = 3.6 V	V _I = V _{CC}		2 1				. 1	μA uO.
	Data inputs	VCC = 3.6 V	V _I = 0	Or tony	K	-5				
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V		5	0 - 3/1	and test	errates da	±100	μΑ
m 08-	Data insula	V 0.V	V _I = 0.8 V	750	70 ×	r(V) se	75	uo ami	de Jud	uO.
I(hold)	Data inputs	VCC = 3 V	V _I = 2 V	-75	es) au	ance, (-75	armert	epsels	μА
lozh		V _{CC} = 3.6 V,	V _O = 3 V		Tierri	5			5	μΑ
lozL	10°68	V _{CC} = 3.6 V,	V _O = 0.5 V		· v pl	-5	en emi	втодть	-5	μΑ
lozpu	sara stresa ratingi operating conditio	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	= 0.5 V to 3 V,	epeiller mu Beer opeil	e moxim or any o	±100*	abnu ba dayloe	tross list on of the	±100	μΔ
lozpd	ratings are observ	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = \frac{V_{CC}}{OE} = \frac{1.5 \text{ V to 0, V}_{O}}{OE} = 1.$	= 0.5 V to 3 V,	ord agolds	ed cone	±100*	r huqiuo	ostis of c tens lugin	±100	μА
			Outputs high	ri basetus	lan si en	0.19	Burthartt	spakego	0.19	
Icc		$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low			5			5	m/
		VI - VCC OF GIVE	Outputs disabled	M eas)	anolli	0.19	enting	ego bi	0.19	nmo
Δlcc [‡]	MY4LVTH16541	V _{CC} = 3 V to 3.6 V, Or Other inputs at V _{CC} or	ne input at V _{CC} – 0.6 V, GND			0.2			0.2	m/
Ci		V _I = 3 V or 0			4			4		pF
Co		V _O = 3 V or 0		-	9			9		pF

^{*}On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH16541, SN74LVTH16541 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS691C - MAY 1997 - REVISED APRIL 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

	16	rear	5	SN54LVTH16541				SN74LVTH16541					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V VCC		2.7 V	UNIT	
	02420		MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
tPLH		Y	1	3.7	42	4	1	2.4	3.5		3.8		
tPHL	Α	Ť	1	3.7	14	4	1	2	3.5	7	3.8	ns	
^t PZH	ŌĒ	Y	1.1	4.8	4	5.7	1.2	2.7	4.6	LOA	5.5	-	
tPZL	OE	T	1.1	4.8	Q.	5.4	1.2	2.8	4.6		5.2	ns	
t _{PHZ}	0.5	9 Y	2.1	6.2		6.5	2.2	4.1	5.9		6.2		
tPLZ	ŌĒ	1	1.9 5.7		6		2.2	3.8	5.4	5.5		ns	
tsk(o)‡	/	J.N		S.	17/21/2		Var	V -	0.5	Y 8.1 3	0.5	ns	

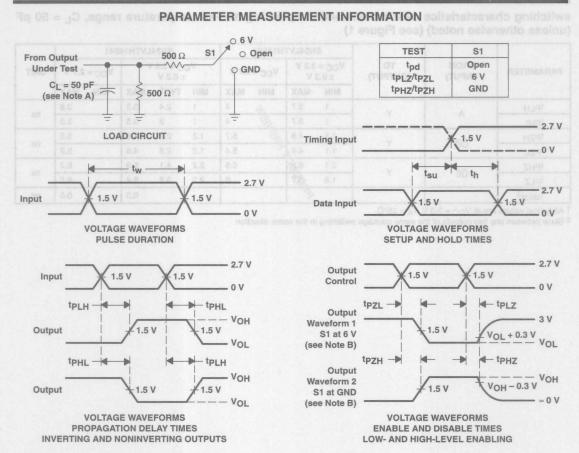
[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

 Toput
 1.5 V
 1.5 V
 1.5 V
 2.7 V
 Contract
 2.7 V
 Contract
 2.7 V
 Contract
 2.7 V
 2.7 V

Toure 1. Load Circuit and Voltage Waveforms

[‡] Skew between any two outputs of the same package switching in the same direction

SCBS691C - MAY 1997 - REVISED APRIL 1998



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_f \leq 2.5 \,$ ns, $t_f \leq 2.5 \,$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH162541, SN74LVTH162541 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS690D - MAY 1997 - REVISED MAY 1998

•	Members of the Texas Instruments Widebus™ Family		TH162541	D	WD PACKA	
WO	Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required		1 <u>OE1</u> [TOP V	48 1 0 10 10 10 10 10 10 10 10 10 10 10 10 10	
•	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation		1Y2 [GND [1Y3 [1Y4 [3 4 5	46 1A2 45 GND 44 1A3 43 1A4	
•	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})		V _{CC} [1Y5 [1Y6 [7	42 V _{CC} 41 1A5 40 1A6	
•	Support Unregulated Battery Operation Down to 2.7 V		GND [1Y7 [11	39 GND 38 1A7	
•	and Pawer Dawn		1Y8 [2Y1 [13	37 1A8 36 2A1	
•	OOV - W OOV T OFFO		2Y2 GND C	15	35 2A2 34 GND 33 2A3	
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors		2Y4 [V _{CC} [2Y5 [17 18	33 2 2A3 32 2A4 31 V _{CC} 30 2A5	
•	Power Off Disables Outputs, Permitting Live Insertion		2Y6 [GND [20	29 2A6 28 GND	
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise		2Y7 [2Y8 [22	27 2A7 26 2A8	
•	Flow-Through Architecture Optimizes PCB Layout		20E1	24	25 2 OE 2	
•	Latch-Up Performance Exceeds 500 mA Per JESD 17					
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)					
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings					

These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

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description

SCBS690D - MAY 1997 - REVISED MAY 1998

description (continued)

The outputs, which are designed to source or sink up to 12 mA, include equivalent $22-\Omega$ series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

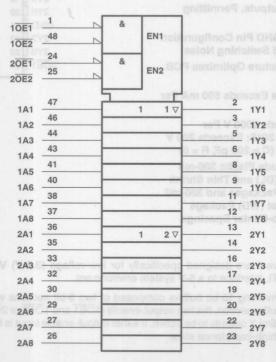
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH162541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH162541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

	INPUTS		OUTPUT
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	High
Н	X	X	Z
X	Н	X	Z

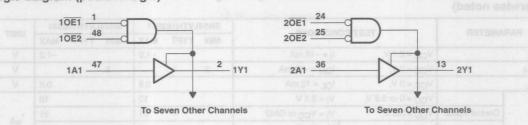
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic) 18-8-11 galls 1940 belong model



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	V ₁ or V _Q = 0 to 4.5 V	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		
Voltage range applied to any output in the h	nigh-impedance	
or power-off state, Vo (see Note 1)		
Voltage range applied to any output in the h	nigh state, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, IO		30 mA
Current into any output in the high state, IO		
Input clamp current, IIK (VI < 0)		
Output clamp current, IOK (VO < 0)		
Package thermal impedance, θJA (see Note	e 3): DGG package	89°C/W
	DL package	94°C/W
Storage temperature range, T _{stq}		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

No. 1819					SN54LVTH	162541	SN74LVTH	162541	LINUT
					MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage				2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage	10	exalifi	LATPENS	2	2	2		V
VIL	Low-level input voltage	= 2.7 V	Nov	V 6.6 = 0.0 V	OY	0.8	18097	0.8	V
VI	Input voltage			W. Walter Co.	Tro-mot	5.5	(10-90)	5.5	٧
ЮН	High-level output current	70400	7076	SAM YAM	1	-12		-12	mA
loL	Low-level output current			0.0	1 25	12	A	12	mA
Δt/Δν	Input transition rise or fall rate	- C.F	Outpu	uts enabled	00	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate	6.0	10.1	504 807	200		200		μs/V
TA	Operating free-air temperature	- Pro		1-2	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN54LVTH162541, SN74LVTH162541 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS			LVTH162	2541	SN74	LVTH16	2541	LINUT
PAI	RAMETER	TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	V
Vон	rys -	V _{CC} = 3 V,	I _{OH} = -12 mA	2		-	2	E (A)		V
VOL		V _{CC} = 3 V,	I _{OL} = 12 mA			0.8			0.8	٧
TE BI		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10			10	
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	ar Chami	STEEL CHEE	±1			±1	μА
1		V 26V	V _I = V _{CC}			1			1	μА
	Data inputs V _{CC} = 3.6 V V _I = 0		gonia, t	190 19	-5	HIST	mane	-5		
loff	V20-	V _{CC} = 0, V _I or V _O = 0 to 4.5 V		±100	μА					
Luc va Doto inputo		V 2V	$V_{l} = 0.8 \text{ V}$ $V_{l} = 2 \text{ V}$		Trail	1 998	75	GET SEE	slov 10	anl.
I(hold) Data inputs		ACC = 3 A			i durale	ynard	-75	ja ogni	age re	μА
lozh	8.0	V _{CC} = 3.6 V,	V _O = 3 V	1	1 1901/1	5	V .etal	a flo-18	5	μА
lozL	DOY OF V B.O-	V _{CC} = 3.6 V,	V _O = 0.5 V	in shir	O.dine	-5	Daliq	nge aç	-5	μА
lozpu		V _C C = 0 to 1.5 V, V _O = OE = don't care	= 0.5 V to 3 V,	0 %	high st	±100*	nidine onibni	to any	±100	μА
lozpd		V _{CC} = 1.5 V to 0, V _O : OE = don't care	= 0.5 V to 3 V,		±100*		t Insmuo omal±10		±100	μА
WALT GO			Outputs high	DION D	DEJ AL	0.19	eqan i	BHHAN	0.19	3571
Icc		$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low			5			5	mA
		AL = ACC OF CHAP	Outputs disabled		Big	0.19	0.19			
Δlcc [‡]	operating condition	V _{CC} = 3 V to 3.6 V, Or Other inputs at V _{CC} or	ne input at V _{CC} - 0.6 V,	liner cond	mozna en In yns 10	0.2	abnu ba devise	ent to mó	0.2	mA
Ci	rieado ena aprillar.	V ₁ = 3 V or 0	s Judni eril ti bisbesoxe ed vi	ni amalia	4	evilspa	Juntary)	4	ort .	pF
Co	THE PERSON	V _O = 3 V or 0	High state and Volv Voc-	16 to 61	9	narte (no evid	9	2. This	pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

V		2 3	S	SN54LVTH1625		1162541 SN74LVT			LVTH16	2541	right	Vist
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.		V _{CC} =	2.7 V		CC = 3.3 ± 0.3 V	V	V _{CC} =	2.7 V	UNIT
4m Ct			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
t _{PLH}	A S		1.1	4.3	4	4.9	1.2	2.9	4.1	vin laved	4.7	112
tPHL the	A	1	1.1	4.3	19	4.9	1.2	2.4	4.1	(Konost A	4.7	ns
tPZH	OOOE	Y	1.4	5.3	24	6.3	1.5	3.2	5		6.1	ns
tPZL	OE	22	1.4	5.1	Q.	5.8	1.5	3.3	4.8	and an arbitrar	5.5	ns
tPHZ	Ted OE	V	2.1	6.1	4 - 57	6.4	2.2	4.3	5.9		6.2	70
tPLZ	OE	Parity and sale take	2.1	5.7	sun stuta	5.9	2.2	4	5.4	E to see	5.5	ns
tsk(o)§				Q.					0.5		0.5	ns

 $^{^{\}dagger}$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

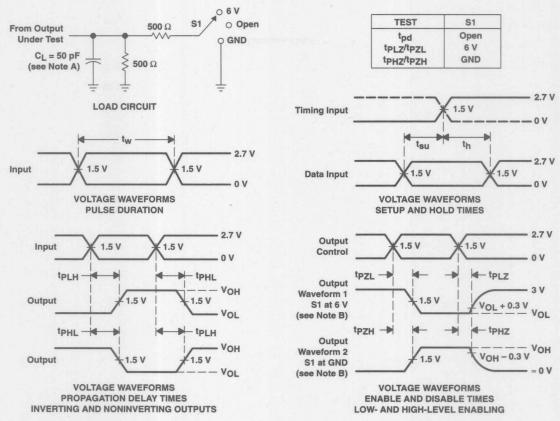


[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[§] Skew between any two outputs of the same package switching in the same direction

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PARAMETER MEASUREMENT INFORMATION

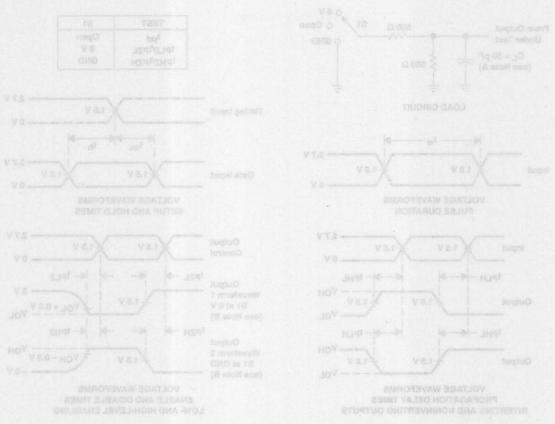


NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- OTES: A. O, Includes probe and ity capacitano
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- and the second the government of the second second
 - as the state of th

Floring 1. Load Clinarill and Voltage Waysforms



SN54LVTH16543, SN74LVTH16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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	Members of the Texas Instruments Widebus™ Family	SN7	SN54LVTH1 74LVTH16543	3 D	WD PACKAGE GG OR DL PACKAGE
own.	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation		1OEAB [1LEAB [1CEAB [1 2	56 1 10EBA 55 1 1LEBA 54 1 1CEBA
.0•8	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})		GND [53 GND 52 1B1
•	Support Unregulated Battery Operation Down to 2.7 V		1A2 [V _{CC} [51 1B2 50 V _{CC}
•	High-Impedance State During Power Up and Power Down		1A3 [1A4 [9	49 1B3 48 1B4
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors		1A5 [GND [1A6 [11 12	47] 1B5 46] GND 45] 1B6
•	Power Off Disables Outputs, Permitting Live Insertion		1A7 [1A8 [2A1 [14	44 1 1B7 43 1B8 42 2B1
•	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C		2A2 [2A3 [16	41 2B2 40 2B3
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise	aval before is were est	GND [2A4 [19	39 GND 38 2B4
•	Flow-Through Architecture Optimizes PCB Layout		2A5 [2A6 [21	37 2B5 36 2B6
•	Latch-Up Performance Exceeds 500 mA Per JESD 17		V _{CC} [2A7 [2A8 [23	35 V _{CC} 34 2B7 33 2B8
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)		GND [2CEAB [2LEAB [25 26	32 GND 31 2CEBA 30 2LEBA
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings		20EAB		29 2OEBA

description

The 'LVTH16543 devices are 16-bit registered transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (\overline{LEAB}\) or \overline{LEAB}\) and output-enable (\overline{OEAB}\) or \overline{OEBA}\) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

Widebus is a trademark of Texas Instruments Incorporated.



SN54LVTH16543, SN74LVTH16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16543 is characterized for operation from –40°C to 85°C.

FUNCTION TABLET (each 8-bit section)

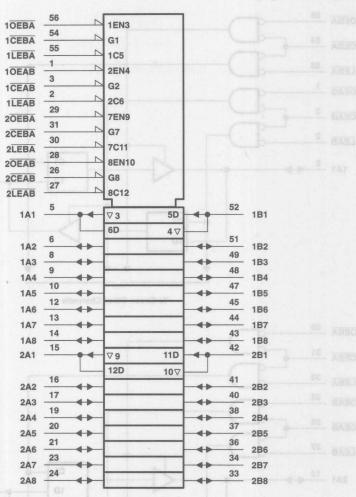
	INPL	JTS		OUTPUT
CEAB	LEAB	OEAB	Α	В
H	Х	X	X	Z
X	X	Н	X	Z
L	Н	L	X	B ₀ ‡
L	L	L	L	L
L	L	L	Н	H

A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

Output level before the indicated steady-state input conditions were established

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logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic) 10EBA 56 1CEBA 54 1LEBA 55 08.80 10EAB 1 FI 570 52 1CEAB 3 1LEAB 2 C1 1A1 5 52___1B1 1D C1 1D To Seven Other Channels 20EBA 29 2CEBA 31 2LEBA 30 20EAB 28 2CEAB 26 2LEAB 27 C1 2A1 15 1D C1

To Seven Other Channels

1D

SN54LVTH16543, SN74LVTH16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, Vo (see Note 1)	
Voltage range applied to any output in the high state, Vo (se	e Note 1)0.5 V to V _{CC} + 0.5 V
Current into any output in the low state, Io: SN54LVTH1654	3 96 mA
SN74LVTH1654	3 128 mA
Current into any output in the high state, Io (see Note 2): Sh	N54LVTH16543 48 mA
SI	N74LVTH16543 64 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, IOK (VO < 0)	
Package thermal impedance, θ _{IA} (see Note 3): DGG packa	
	74°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

	75	75	V8.0=/V1	SN54LVT	H16543	SN74LVT	H16543	LIMIT
				MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		,5 V to 3 V,	OV 2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage			2	12	2		٧
VIL	Low-level input voltage		V5 V to 3 V.	0V .001 V	8.0	V	0.8	٧
VI	Input voltage			8	5.5		5.5	٧
ЮН	High-level output current		udiu smybnis	N	-24	V: .	-32	mA
loL	Low-level output current		ALON SULCIDIO 4	25	48	2	64	mA
Δt/Δν	Input transition rise or fall rate		Outputs enabled	0	10		10	ns/V
Δt/ΔVCC	Power-up ramp rate		St. orn – COSA se andui	200	V = 0:	200		μs/V
TA	Operating free-air temperature			-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN54LVTH16543, SN74LVTH16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS699C - JULY 1997 - REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

VVest	(2.0		UD ITTO A LOCAL DE LA CALLACTE DE LA	SN5	4LVTH1	6543	SN74	4LVTH16	6543	ord
PAI	RAMETER	TEST CO	NDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	רואט
VIK	-0.5	V _{CC} = 2.7 V,	I _I = -18 mA		F stoid	0-1.2	tate, V	s flo-re	-1.2	V
18.0+	O.S V to Voc	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0	.2	any o	VCC-0.	2	age ra	loV -
km 80		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4	ISAS WO	l ent n	2.4	YAS CI	ni Iner	V
VOH		V OV OBSTOALS	I _{OH} = -24 mA	2						V
Am 84		VCC = 3 V S 128 7 147	I _{OH} = -32 mA	Ol Sam	Or various ulbu enn un andu 5 A	VIIID OI	III allert	U.J.		
Am 08-		V07V	I _{OL} = 100 μA		1	0,2	sul trui	mun m	0.2	bonl
		V _{CC} = 2.7 V	I _{OL} = 24 mA		(0 >	0.5	i toan	Bo ami	0.5	uO.
MO-18			I _{OL} = 16 mA	e Note	ea) ALS	0.4	l Imped	armad	0.4	s9 _V
VOL		V-2-2V	I _{OL} = 32 mA			0.5			0.5	V
		VCC = 3 V	I _{OL} = 48 mA		or pr	0.55	ist etub	впрага	rage te	Std
ore vine		amenge to the dayles. These	I _{OL} = 64 mA	aprilles mu	misem o	gh ads"	iobau ba	hose list	0.55	28280
on el "en	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	har son	g sny pl	4 ±1	noiveb a	arti to rici	15 18±1	anoilo
	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	o manaha	24	10	Katanafa yay 1	Ottober OF I	10	bello see
lį			V _I = 5.5 V	Lett ni si	RITA O SI	20	lno awel	finemus	20	μΑ
	A or B ports‡	V _{CC} = 3.6 V	VI = VCC	ni betetu	3	nebeq1	farmarti	seckage	Set The	
175.5			V ₁ = 0	, c	3	-5	5		-5	
loff		$V_{CC} = 0$, V_I or $V_O = 0$ to	4.5 V	Q	452157121	1313133	Battista a	ada n	±100	μΑ
II(hold)	A or B ports	V _{CC} = 3 V	V _I = 0.8 V	75			75			μА
'I(noid)	A of B ports	ACC - O A MINI	V ₁ = 2 V	-75			-75			μΛ
IOZPU	2,7 3,6	$\frac{V_{CC}}{OE} = 0 \text{ to } 1.5 \text{ V}, V_{O} = 0$ OE = don't care	.5 V to 3 V,			±100*	et aut volter		±100	μА
lozpo	8.0	$\frac{\text{V}_{CC}}{\text{OE}} = 1.5 \text{ V to 0, V}_{O} = 0$.5 V to 3 V,			±100*	pallov ha	gal tevel	±100	μА
Am	56-	V _{CC} = 3.6 V,	Outputs high	-	(1000)000000000000000000000000000000000	0.19	no en frants	as laugh	0.19	- Interest
Icc		I _O = 0,	Outputs low			5	cours have	ten laund	5	m/
VAnn	OF .	V _I = V _{CC} or GND	Outputs disabled	-		0.19	so pails of	illiansey!	0.19	146
			CC = 3 V to 3.6 V, One input at VCC - 0.6 V, her inputs at VCC or GND			0.2	eter on	181 QU-10	0.2	_ mA
Ci	08	V _I = 3 V or 0		-	4	prenatoria	1100 100-0	4	ndo	pF
Cio	assings it entrol	V _O = 3 V or 0	tout and a division of a	A SHOTE GO	10	THE CHI	O SOUQUITY	10	Nacillary	pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

 $^{^{\}dagger}$ All typical values are at VCC = 3.3 V, TA = 25°C. ‡ Unused pins at VCC or GND

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

18	TEST		9	SN54LV	TH16543	18	Canan S	SN74LV	TH16543		
			V _{CC} =		V _{CC} =	V _{CC} = 2.7 V		3.3 V 3 V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	SP CONTRACT
t _W Pulse duration, L	Pulse duration, LEAB or LEBA low		3.3		3.3		3.3		3.3		ns
	A or B before	Data high	0.5		9.5		0.5	-	0.5		200
constitution of the 2.7 V	LEAB↑ or LEBA↑	Data low	0.8		1.3		0.8		1.3	T- IT	ns
t _{su} Setup time	A or B before	Data high	0		0		0	of Miles	0	1341	no
	CEAB↑ or CEBA↑	Data low	0.6	6	1.1		0.6	7	1.1		ns
- 3	A or B after	Data high	1.5	3	0.7		1.5	190	0.7		
h Hold time	LEAB↑ or LEBA↑	Data low	1.2	013	1.3		1.2		1.3		ns
th Hold time	A or B after	Data high	1.7	Q.	0.9	was A	1.7	A P	0.9		no
A O moreover, James and	CEAB↑ or CEBA↑	Data low	1.6		1.8		1.6		1.8		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

	VERY	1818	ugla0 s	N54LV	TH16543			SN74	LVTH16	6543	31,100		
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 \		V	Vcc=	V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
t _{PLH}	A or B	P or A	1.1	3.4	1003	3.9	1.2	2.3	3.2	E	3.7	One	
tPHL -	AOFB	B or A	3 01.1 0	3.4	Jo	3.9	1.2	2.1	3.2	-	3.7	ns	
tPLH SHE	-M LE	A or B	1.2	4.1	2	5.1	1.3	2.5	3.9	Dr- nas	4.9	ns	
^t PHL	LE	AOIB	1.2	4.1	54	5.1	1.3	2.3	3.9		4.9	115	
tPZH - H	1.5 Y Y Z	Asse	1.2	4.5	2	5.6	1.3	2.8	2.8 4.3		5.4		
V 0 tPZL	ŌĒ	A or B	1.2	4.5	A 30	5.6	1.3	2.8	4.3		5.4	ns	
tPHZ	WAVE CORMS	A or B	1.9	4.9	5	5.4	2	3.5	4.7	Liov	5.2		
tPLZ	OE A	AOFB	1.9	4.6		4.7	2	3.3	4.4	PROPA	4.5	ns	
tPZH ***	LIUANS JSV3.)-1	A an P	1.2	4.7		5.8	1.3	3	4.5	NA SAME	5.6		
tPZL	CE	A or B	1.2	4.7		5.8	1.3	3	4.5	rebulors	5.6	ns	
tPHZ 1	dissibled by the or	site toecore viol s	1.9	5.1	Nas anoshi	5.6	2	3.6	4.9	i moss	5.4		
tPLZ	ent vo CEldasib r	A or B	1.9	4.9	on and receive	5.1	2	3.5	4.7	State Turns	4.9	ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

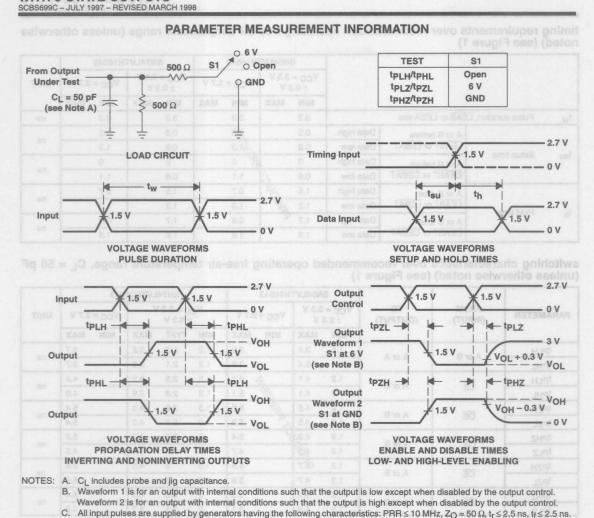


Figure 1. Load Circuit and Voltage Waveforms

D. The outputs are measured one at a time with one transition per measurement.

SN54LVTH16646, SN74LVTH16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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	Members of the Texas Instruments <i>Widebus</i> ™ Family	SN54LVTH1 SN74LVTH1664	3		PACKAG		
	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation	1DIR [1 2	56 55	1CLKBA	pur-si	
•	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V VCC)	1SAB GND 1A1 1A2 1A2	4 5	53	1SBA GND 1B1 1B2		
•	Support Unregulated Battery Operation Down to 2.7 V	V _{CC} l	7	50 49	V _{CC} 1B3		
	High-Impedance State During Power Up	1A4 l 1A5 l GND l	10	47	1B4 1B5 GND		
	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C	1A6 [12	45	1B6		
	Bus Hold on Data Inputs Eliminates the Month Control Need for External Pullup/Pulldown Resistors	1A8 (2A1 (2A2 (14 15	43 42	1B8 2B1 2B2		
	Power Off Disables Outputs, Permitting Live Insertion	2A3 [17	40	2B3		
	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise	2A4 2A5	20	37	2B4 2B5		
	Flow-Through Architecture Optimizes PCB Layout	2A6	22	35	2B6 V _{CC}		
	Latch-Up Performance Exceeds 500 mA Per July 150 JESD 17	2A7 [2A8 [GND]	24	33	2B7 2B8 GND		
	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)	2SAB [2CLKAB [26 27	31 30	2SBA 2CLKBA	H	
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package	2DIR [28	29	2 <u>0E</u>		

description

The 'LVTH16646 devices are 16-bit bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH16646 devices.

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Using 25-mil Center-to-Center Spacings



SN54LVTH16646, SN74LVTH16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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description (continued)

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE}) high). A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16646 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

					10	HOHOH HADEL		
		INPL	JTS T	EAS		DAT	A I/O	O selection on Function
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OPERATION OR FUNCTION
X	X	38 J 1B4	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	1	X	X	Unspecified†	Input	Store B, A unspecified†
Н	X	00 ↑ 1 00	1	X	X	Input	Input	Store A and B data
Н	X	HorL	HorL	20 X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	HorL	X	Н	Output	Input	Stored B data to A bus
L	Н	ABEXTIE	X	BARL	X	Input	Output	Real-time A data to B Bus
L	HA	HorL	X	SCH KAB	X	Input	Output	Stored A data to bus

[†] The data-output functions may be enabled or disabled by various signals at $\overline{\text{OE}}$ or DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.



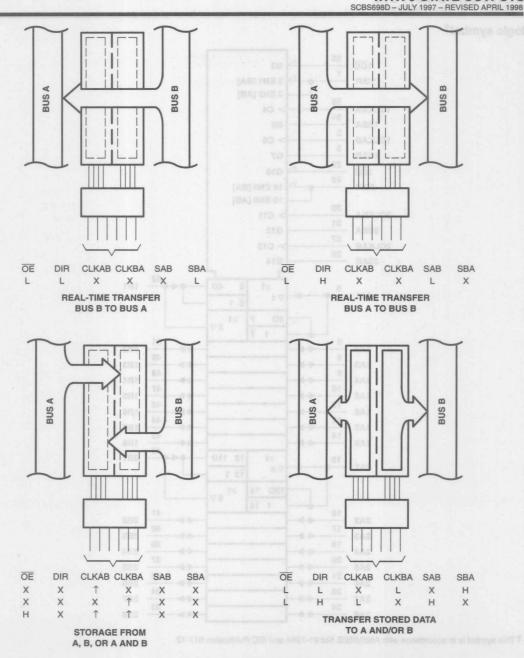
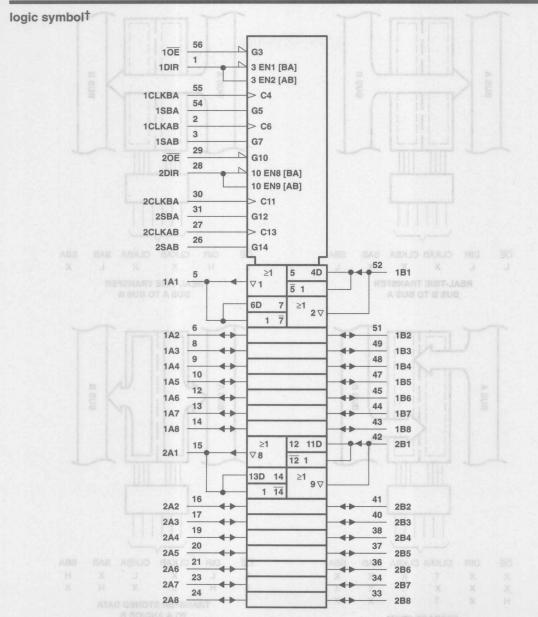


Figure 1. Bus-Management Functions

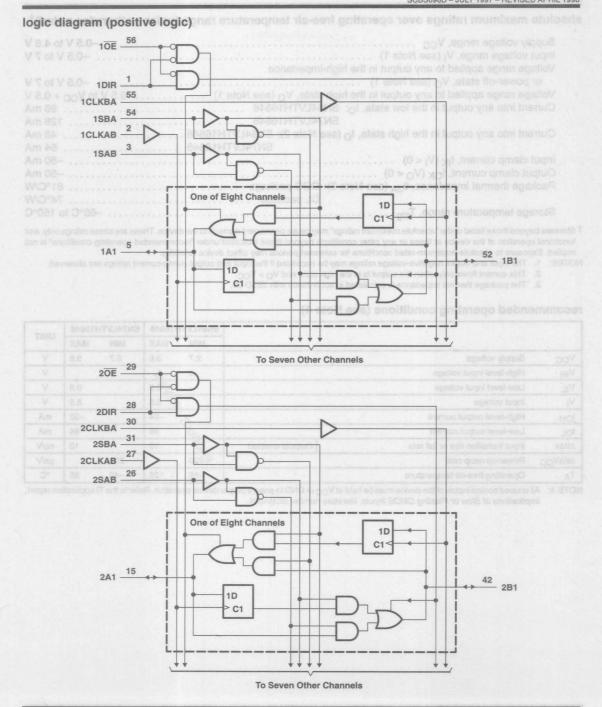


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[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high-impedance	
or power-off state, VO (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, Vo (see Note 1)	
Current into any output in the low state, Io: SN54LVTH16646	96 mA
SN74LVTH16646	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVTH16646	48 mA
SN74LVTH16646	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, IOK (VO < 0)	
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVTI	116646	SN74LVTI	H16646	LINUT
		* * * *	MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	To Sayen Other Channels	2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	4	2		٧
VIL	Low-level input voltage			6.8		0.8	٧
VI	Input voltage			5.5	88	5.5	٧
ЮН	High-level output current		1	-24	Tie Male	-32	mA
loL	Low-level output current		3	48	- A60	64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	0	10	AGE	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	d · l	2200	-5	200	201.1	μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.





electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	THIT BASS	BALAST	Maara erry, mana error	SN54	LVTH1	6646	SN74	4LVTH1	6646	
PA	RAMETER	VER WOOV TEST C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2		all s	-1.2	٧
	XAM HIM	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	VCC-0.	2		VCC-0	.2		
sHM.		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4		2.4			V	
VOH		v	IOH = -24 mA	2		Wol 10	allu sere	, notino	b sulur)	V
		V _{CC} = 3 V	I _{OH} = -32 mA	igin etro	4		2	,em	Setup ti	
	8,8	V - 07V	I _{OL} = 100 μA	wed the		0.2	D TOPIAL	in plate	0.2	
		V _{CC} = 2.7 V	I _{OL} = 24 mA	ala nigh	1	0.5	-	(6)	0.5	
		5.0	I _{OL} = 16 mA	WOI BISE		0.4	NO POPO	ADD TOTAL	0.4	1/
VOL			I _{OL} = 32 mA			0.5			0.5	V
		V _{CC} = 3 V	I _{OL} = 48 mA	DIESCINE	0091	0.55	Others	110516	na ga	
			I _{OL} = 64 mA	12.0	· Paragraphic states and states a			0.55		
	3)489	V _{CC} = 3.6 V,	V _I = V _{CC} or GND		Š	£1			±1	
TRID	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	YOU	24	10	MO	89	10	
		FARE TOWN 1885	V _I = 5.5 V		Y. Carrie	20	110	1914)	20	μΑ
	A or B ports‡	V _{CC} = 3.6 V	VI = VCC		3	1			1	
	150	150	V _I = 0	0	ř	-5			-5	
loff	1.2	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V	Q	8 10	A	10 AE		±100	μА
La ca	A su D words	War OV	V _I = 0.8 V	75			75		-	
I(hold)	A or B ports	VCC = 3 V	V _I = 2 V	-75	A to	9	-75	A		μΑ
lozpu	5.9 5.4	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	= 0.5 V to 3 V,		0.00	±100*	TOAGA	A 882	±100	μА
lozpo	5.4	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{OE} = \frac{V_{CC}}{OE} = \frac{1.5 \text{ V to 0, V}_{OE}}{V_{OE}} = 1.5 \text$	= 0.5 V to 3 V,			±100*			±100	μА
611	8.2	1 2.6 6.0	Outputs high	2	0,10	0.19	311	2	0.19	cel
Icc		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs low	8		5			5	mA
		Al = ACC of GMD	Outputs disabled	8	0.10	0.19			0.19	
Δlcc§	6.8	V _{CC} = 3 V to 3.6 V, On Other inputs at V _{CC} or	ne input at V _{CC} - 0.6 V,		E 10	0.2	FI	O	0.2	mA
Ci	AA .	V _I = 3 V or 0	15 0	2	4			4		pF
Cio	7.3	V _O = 3 V or 0		2 5	10	4	P81	10		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ Unused pins at V_{CC} or GND

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

	HIEGGE SNYALVINISSAS	TVJASNO	SN54LVTH16646				5				
				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		3.3 V	V _{CC} = 2.7 V		UNIT
					ALT ME IN R. B.		± 0.3 V				
	CO-NeV	S.O-GaV	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			150	- 3491	150	VTR	150		150	MHz
t _W	Pulse duration, CLK high or low		3.3	Am July	3.3		3.3		3.3		ns
	Setup time,	Data high	1.2	Anisk	1.5		1.2	204	1.5		
tsu	A or B before CLKAB↑ or CLKBA↑	Data low	2	100 X	2.8		2		2.8		ns
	Hold time,	Data high	0.5	19	0		0.5	DOV	0		
th	A or B after CLKAB↑ or CLKBA↑	0.5	Am 85	0.5		0.5		0.5	Land.	ns	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

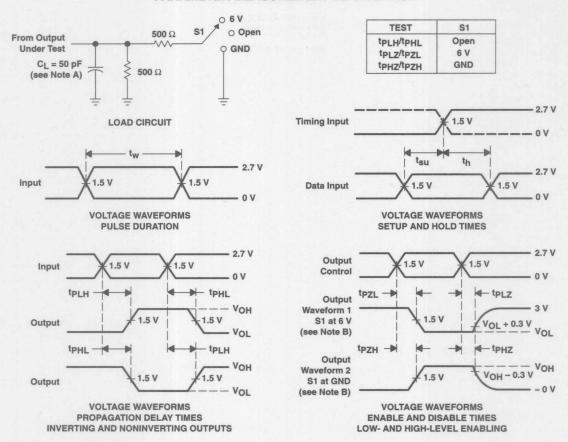
T±				SN54LV	TH16646	V = IV		SN74	LVTH16	6646		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.		V _{CC} =	2.7 V	V _{CC} = 3.3 ± 0.3 V		V	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
fmax			150		150	Charles AV	150			150		MHz
tPLH	CLKBA or	A or B	1.3	4.5		5	1.3	2.8	4.2		4.7	ns
t _{PHL}	CLKAB	AOIB	1.3	4.5	V/A	5	1.3	2.8	4.2		4.7	115
tPLH	A or B	B or A	1	3.6		4.1	1	2.4	3.4	ahoq (3.9	ns
t _{PHL}	AOFB	BOTA	1	3.6	5	4.1	1,	2.1	3.4		3.9	115
tPLH	ODA OADT	A or B	1	4.7	13	5.6	1	2.8	4.5		5.4	ns
tPHL	SBA or SAB‡	AOFB	1	4.7	V V St	5.6	ov.1	3	4.5		5.4	115
^t PZH		A or B	1	4.5		5.4	1	2.5	4.3		5.2	ns
tPZL	ŌĒ	AOIB	1	4.5	rigiri at	5.4	1	2.6	4.3		5.2	115
tPHZ		A or B	2	5.8	Wol at	6.3	2	4	5.6	in the second	6.1	ns
tPLZ	ŌĒ	A OF B	2	5.6	idealb at	6.3	2	3.6	5.4		6.1	115
tPZH	DIR	A or B	1	4.6	- 00V B	5.5	0.71	1 V 3	4.4		5.3	ns
tPZL	DIR	AOIB	1	4.6		5.5	1	3	4.4		5.3	115
tPHZ	DIR	A or B	1.5	6	Per Jacob Anton	7.1	1.5	3.9	5.7		6.8	ne
tpLZ	Of DIR	AOLB	1.5	5.5		6	1.5	3.6	5.2		5.7	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] These parameters are measured with the internal output state of the storage register opposite that of the bus input.

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PARAMETER MEASUREMENT INFORMATION

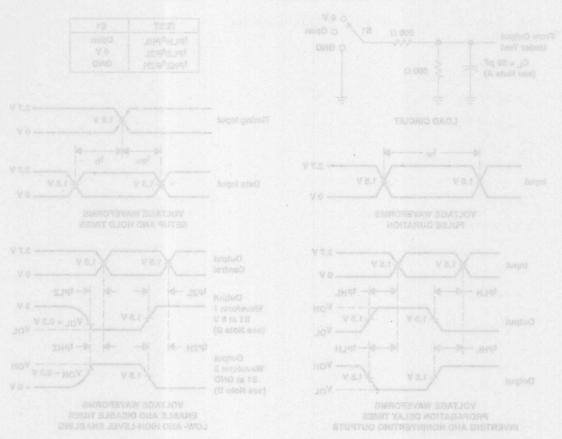


NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O}=50~\Omega,\,t_{f}\leq$ 2.5 ns, $t_{f}\leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Cr. Includes probe and lig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All locut pulses are supplied by generators having the following characteristics: PFR ≤ 10 MHz, ZQ = 50 Ω, t ≤ 2.5 ns, t ≤ 2.5 ns
 - The minute are reasonable one at a time with one transition are measurement. Of

Figure 2. Load Circuit and Voltage Waveforms



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•	Members of the Texas Instruments Widebus™ Family	SN54LVTH16652 WD PACKAGE SN74LVTH16652 DGG OR DL PACKAGE (TOP VIEW)								
•	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V		10EAB [1	10EBA				
	Operation and Law Static Dower		1CLKAB	3] 1CLKBA	ura. Hral			
	Dissipation		1SAB		100000	1SBA				
	Support Mixed-Mode Signal Operation		GND			GND				
	(5-V Input and Output Voltages With		1A1 [5	52	1B1				
	3.3-V V _{CC})		1A2 [6	51	프린테 전문 손들이				
	Support Unregulated Battery Operation			7	591 11 227	Vcc				
	Down to 2.7 V		1A3 [THE REAL PROPERTY.	49	The second second				
	High-Impedance State During Power Up		1A4 [9	48	1B4				
	and Power Down		1A5 [10	47	1B5				
			GND [11	46	GND				
	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C		1A6 [12	45] 1B6				
			1A7 [13	44] 1B7				
	Bus Hold on Data Inputs Eliminates the		1A8 [14	43] 1B8				
	Need for External Pullup/Pulldown		2A1 [15	42	2B1				
	Resistors Off Blackles Outside Boundary		2A2 [16	41] 2B2				
-	Power Off Disables Outputs, Permitting		2A3 [17	40] 2B3				
	Live insertion		GND [18	39	GND				
-	Distributed V _{CC} and GND Pin Configuration		2A4 [19	38] 2B4				
	Minimizes High-Speed Switching Noise		2A5 [20	1000] 2B5				
	Flow-Through Architecture Optimizes PCB		2A6	21		2B6				
	Layout A bloss and sugar the floor and the f		V _{CC}	22		Vcc				
	Latch-Up Performance Exceeds 500 mA Per		2A7		Contract Contract	2B7				
	JESD 17 3 and last? Manual Manual Miglion		2A8			2B8				
	ESD Protection Exceeds 2000 V Per			25	32					
	MIL-STD-883, Method 3015; Exceeds 200 V		2SAB	275		2SBA				
	Using Machine Model (C = 200 pF, R = 0)		2CLKAB	3 %	-	2CLKBA	H			
0	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink		20EAB [28	29] 20EBA				
	Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings									

description

The 'LVTH16652 devices are 16-bit bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH16652 devices.

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description (continued)

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last level configuration.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH16652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16652 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

		INP	UTS	AS		DATA	A I/OT	ODERATION OF FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	X	X	Input	Input	Isolation
L	Н	1	1	X	X	Input	Input	Store A and B data
X	Н	1	HorL	X	X	Input	Unspecified [‡]	Store A, hold B
Н	Н	1	1	X‡	X	Input	Output	Store A in both registers
L	X	HorL	1	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	VE TUBE	1	X	X [‡]	Output	Input	Store B in both registers
L	L	X	X	AS X	L	Output	Input	Real-time B data to A bus
L	L	X	HorL	X	Н	Output	Input	Stored B data to A bus
Н	Н	X	X	ALL	Х	Input	Output	Real-time A data to B bus
Н	Н	HorL	X	Н	X	Input (0)	Output	Stored A data to B bus
Н	L	H or L	H or L	Н	н	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

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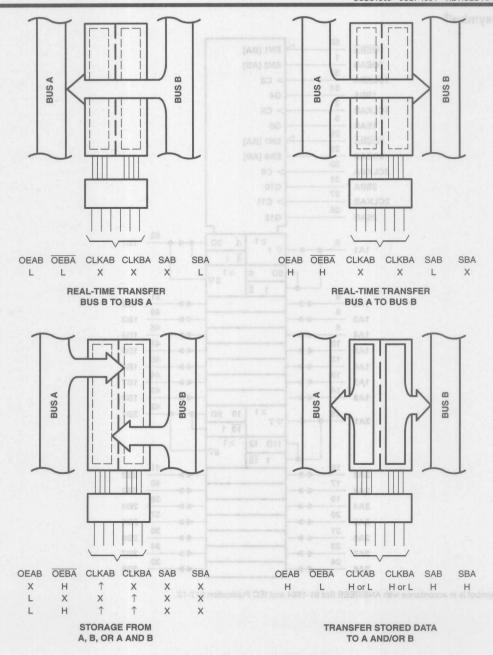
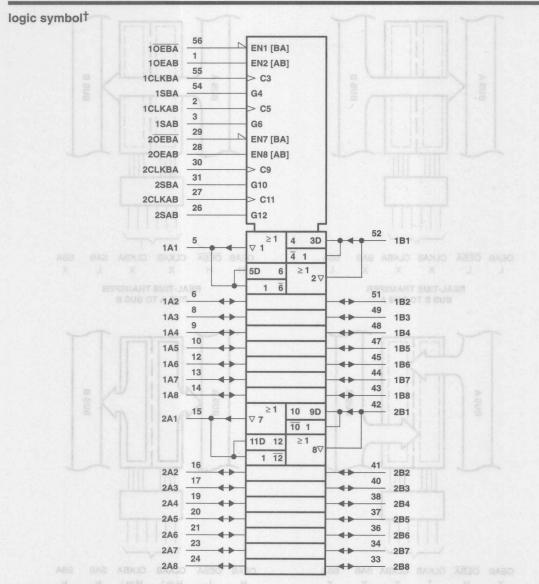


Figure 1. Bus-Management Functions



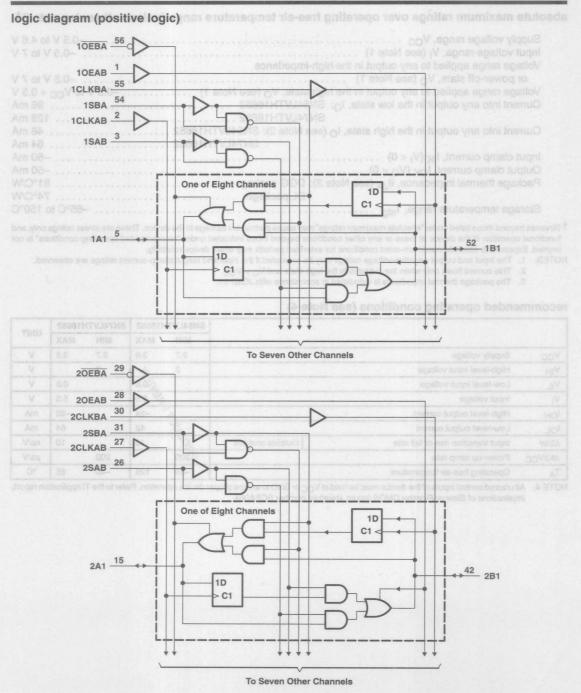
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[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance or power-off state, V _O (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, Vo (see Note 1)	
Current into any output in the low state, Io: SN54LVTH16652	96 mA
SN74LVTH16652	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVTH16652	48 mA
SN74LVTH16652	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

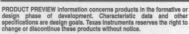
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

				SN54LVTI	H16652	SN74LVT	H16652	LIMIT
				MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	elennario le	To Seven Oth	2.7	3.6	2.7	3.6	V
VIH	High-level input voltage			2	4	2	ős	٧
VIL	Low-level input voltage				8.0		0.8	٧
VI	Input voltage				5.5	BAB	5.5	٧
ЮН	High-level output current			1	-24	SE ARM	-32	mA
loL	Low-level output current	7		130	48	31	64	mA
Δt/Δν	Input transition rise or fall rate		Outputs enabled	0	10	TS GAN	10	ns/V
Δt/ΔVCC	Power-up ramp rate			2200		200		μs/V
TA	Operating free-air temperature			-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.





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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		SHINK	SN54	LVTH1	6652	SN7	UNIT					
		TEST C	MIN	TYPT	MAX	MIN	TYPT	MAX	UNI			
VIK	- 100	V _{CC} = 2.7 V,	I _I = -18 mA		178	-1.2			-1.2	٧		
	XAM MOV.	V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} -0.2			VCC-0					
sidal		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4			2.4	coneups	Clock to	٧		
VOH		V _{CC} = 3 V	I _{OH} = -24 mA	2		well to i		uration,				
			I _{OH} = -32 mA	figliri altaC			2	,smi	Setup t			
	2.8	V _{CC} = 2.7 V	I _{OL} = 100 μA	Sale forc		0.2	D BAND	U enemen	0.2			
			I _{OL} = 24 mA	light staC		0.5			0.5			
		2.0	I _{OL} = 16 mA	. wolverac	0.4				0.4	V		
VOL		W- 0W	I _{OL} = 32 mA			0.5				V		
		VCC = 3 V	I _{OL} = 48 mA	(A 910009) 19 0.55			0.55			rioti:		
			I _{OL} = 64 mA									
	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10			10			
		V _{CC} = 3.6 V,	V _I = V _{CC} or GND	c or GND ±				193	±1			
li	A or B ports‡	V _{CC} = 3.6 V	V _I = 5.5 V	0	1 8	20	(TUS	MI)	20	μА		
			V _I = V _{CC}	54 115	6	1						
	150	160	V _I = 0 001	01 2	2	-5			-5			
loff	4.7	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V	00					±100	μΑ		
lea e a	A or B ports	Vcc = 3 V	V _I = 0.8 V	9 5			75 -75			μΑ		
I(hold)		ACC = 2 A	V _I = 2 V						Н	μ		
lozpu	8.8	$\frac{V_{CC}}{OE/OE} = 0 \text{ to } 1.5 \text{ V, V}_{O} = 0$	= 0.5 V to 3 V,	î l		±100*	9.0		±100	μА		
lozpd	5.4	V _{CC} = 1.5 V to 0, V _O : OE/OE = don't care	= 0.5 V to 3 V,	t de	A 30 2	±100*	ABER	BAB	±100	μА		
ns.			Outputs high		A	0.19	ASS	990	0.19			
lcc		$V_{CC} = 3.6 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low			5			5	mA		
	1.0	11 - 400 or grap	Outputs disabled		A		ASS	10	0.19			
∆lcc§	4.9	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			8	0.2	BAS	10	0.2	m/		
Ci	5.F	V _I = 3 V or 0	1.0	9	4			4		pF		
Cio	2.0	V0 = 3 V or 0	6.0	0	10		200	10	7	pF		

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

 $^{^{\}dagger}$ All typical values are at VCC = 3.3 V, TA = 25°C. ‡ Unused pins at VCC or GND

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

THAU	SNITALVIHIEBSS	SHEALVTH19652		SN54LVTH16652				SN74LVTH16652				Am	
			PT 1984	V _{CC} =		Vcc=	2.7 V	VCC:	= 3.3 3 V	V _{CC} =	2.7 V	UNIT	
		A CONTRACTOR OF THE PARTY OF TH		MIN MAX		MIN MAX		MIN MAX		MIN MAX		281*	
fclock	Clock frequency		2.4		150	* HO!	150	WY.S=	150		150	MHz	
t _W	Pulse duration, CLK high or low			3.3	-24 mA	43.3		3.3		3.3		ns	
	Setup time,		Data high	1.2	Am Sac	1.5		1.2	DDY	1.5		ns	
tsu A or B before CLKAB↑ or C		or CLKBA1	Data low	2	0000	2.8		2		2.8			
th	Hold time,		Data high	0.5	16,	0		0.5	201	0			
	A or B after CLKAB↑ or CLKBA↑ Data low			0.5	Am at	0.5		0.5		0.5		ns	

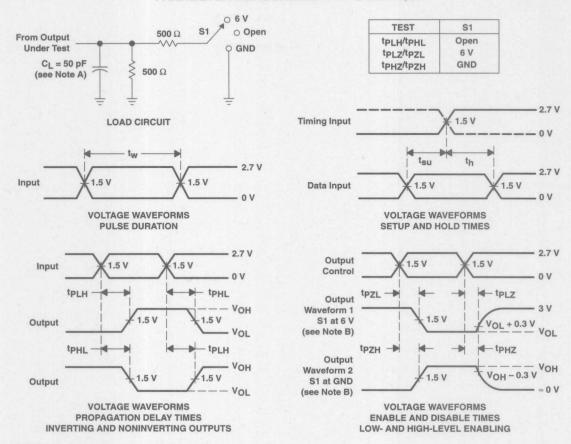
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

101		TO (OUTPUT)	SN54LVTH16652				.VI	Consi					
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V	CC = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
f _{max}		9,	150		150	0=14	150			150		MHz	
tPLH 1	CLK	BorA	1.3	4.5	# 0 = 0 /	5	1.3	2.7	4.2		4.7	Ho	
tPHL		BorA	1.3	4.5	V.S.	5	1.3	2.8	4.2	and the same of	4.7	ns	
tPLH	A or B	A == B	B or A	1	3.6	V	4.1	1	2.4	3.4		3.9	
tPHL		BOLA	1	3.6	1	4.1	oV.1	2.1	3.4		3.9	ns	
tPLH	SAB or SBA	B or A	1	4.7	ii.	5.6	1	2.7	4.5		5.4	ns	
tPHL		BOTA	1	4.7	SC. N.E.	5.6	1	3	4.5		5.4	ns	
^t PZH		A A	1	4.5		5.4	1	2.4	4.3		5.2	ns	
tPZL	OEBA	11,0 A	1	4.5	110010	5.4	0-1	2.3	4.3		5.2	ns	
t _{PHZ}	OFD4	A	2	5.8	ALC: U	6.3	2	3.9	5.6		6.1	200	
tPLZ	OEBA	A	2	5.6	ASSESSED AS	6.3	2	3.4	5.4		6.1	ns	
tPZH 1	OEAB	OFAR B	LO D	1.3	4.4	MA	5.1	1.3	2.7	4.2		4.9	ns
tPZL		В	1.3	4.4		5.1	1.3	2.6	4.2		4.9	ns	
tPHZ	OEAB	В	1.6	5.8		6.5	1.3	3.5	5.5		6.2	ne	
tPLZ	UEAB	В	1.6	5.8	on the latest and	6.5	1.3	3.2	5.5	At the state of	6.2	ns	

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION



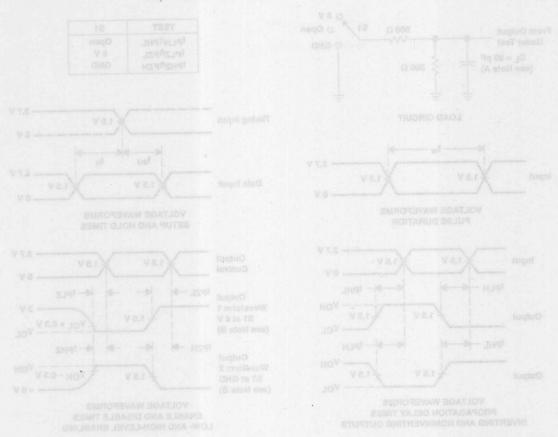
NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. Ot Includes probe and jig especitant a

B. Wavetorm 1 is for an outgot with interest conditions such that the output is now except when disabled by the output control.

Wavetorm 2 is for an output with internal conditions such that the output is night except when disabled by the output control.

D. The outputs are pressured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Wavelorms



SN54LVTH16835, SN74LVTH16835 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS WITH 3-STATE OUTPUTS

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•	Members of the Texas Instruments Widebus™ Family		SN54LVTH16835 WD PACKAGE SN74LVTH16835 DGG OR DL PACKAGE (TOP VIEW)						
•	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation					NC NC Y1	1 2	56 GND 55 NC 54 A1	
•	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})	A				GND [Y2 [Y3]	4 5	53 GND 52 A2 51 A3	
•	Support Unregulated Battery Operation Down to 2.7 V					V _{CC} [7 8	50 V _{CC} 49 A4	
•	High-Impedance State During Power Up and Power Down					Y5 Y6 GND	10	48 A5 47 A6 46 GND	
•	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C					Y7 Y8	12	45 A7 44 A8	
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors					Y9 Y10 Y11	14 15	43 A9 42 A10 41 A11	
•	Power Off Disables Outputs, Permitting Live Insertion					Y12	17	40 A12 39 GND	
•	Distributed V _{CC} and GND Pin Configurate Minimizes High-Speed Switching Noise	ion				Y13 Y14		38 A13 37 A14	
•	Flow-Through Architecture Optimizes PC Layout		V _{CC}	22	36 A15				
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrin Small-Outline (DGG) Packages and 380-n Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings	ık				Y16 Y17 GND Y18 OE LE	24 25 26 27	34	
lesc	cription								

The 'LVTH16835 devices are 18-bit universal bus drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow from A to Y is controlled by the output-enable (OE) input. These devices operate in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of the clock. When OE is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Widebus is a trademark of Texas Instruments Incorporated



NC - No internal connection

SN54LVTH16835, SN74LVTH16835 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS WITH 3-STATE OUTPUTS

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description (continued)

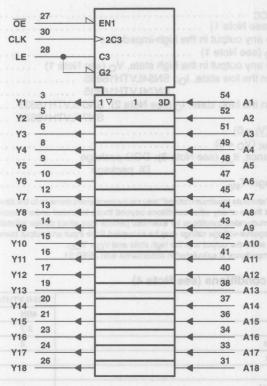
The SN54LVTH16835 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16835 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

	INP	UTS		OUTPUT
OE	LE	CLK	Α	Y
Н	X	X	Χ	Z
L	Н	X	L	L
L	Н	X	Н	Н
L	L	1	L	L
L	L	1	Н	Н
L	L	Н	X	Yot
L	L	L	X	Y0 [‡]

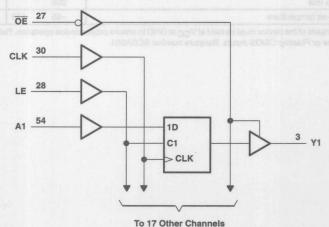
† Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes low

‡ Output level before the indicated steady-state input conditions were established



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH16835, SN74LVTH16835 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)0.5 V to 7 V	
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	
Voltage range applied to any output in the high state, Vo (see Note 1)0.5 V to Vcc + 0.5 V	
Current into any output in the low state, IO: SN54LVTH16835	
SN74LVTH16835	
Current into any output in the high state, IO (see Note 2): SN54LVTH16835	
SN74LVTH16835	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Package thermal impedance, 0,1A (see Note 3): DGG package	
DL package	
Storage temperature range, T _{sta}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and VO > VCC.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

	57 ATG		SN54LVTI	H16835	SN74LVT	H16835	LIMIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage	AND CONTROL OF THE PARTY OF THE	2		2		٧
VIL	Low-level input voltage	name and the second	36	0.8		0.8	٧
VI	Input voltage	- Address of the second	317	5.5		5.5	V
ЮН	High-level output current	Galland OSChara Model	o Les organio	-24	one become	-32	mA
loL	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	del	10	istancia i	10	ns/V
Δt/ΔVCC	Power-up ramp rate		200	7	200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

14-	and Scholer	AND SELECTION OF S	BUTATV INGKE	SN5	4LVTH1	6835	SN74	4LVTH16	6835		
PAI	RAMETER	TEST CON	IDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
VIK		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	٧	
	(Section 2011)	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0	.2	the medical	VCC-0.	2	-	to the same of	
SHM		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4			2.4	Astronia.	A assert	V	
VOH		V 2.V	I _{OH} = -24 mA	2			1 50	notion	Pulse di	V	
		V _{CC} = 3 V	I _{OH} = -32 mA	- was		NO TRAIN	2				
		V 07V	I _{OL} = 100 μA		TVI-25	0.2	SIBCL		0.2		
		V _{CC} = 2.7 V	I _{OL} = 24 mA	taffat sirk	4 13	0.5	alsG.		0.5		
			I _{OL} = 16 mA	V(D) ALA		0.4			0.4	V	
VOL		The second secon	I _{OL} = 32 mA		LA LA	0.5	01801	101	0.5	V	
		VCC = 3 V	I _{OL} = 48 mA			0.55	100 test	-	and the same		
			I _{OL} = 64 mA		EUG JAN				0.55		
of no	To Galani	VCC = 0 or 3.6 V,	V _I = 5.5 V	The state of the s	UUUT.	10	STREET BY		10	Historia Sensole	
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1			±1		
l _l		FMTVJP192	V _I = V _{CC}	-		1			1	μА	
	A inputs	V _{CC} = 3.6 V	V _I = 5.5 V	127	GT COL	20	REC	1272 1240	20		
		7.637	V ₁ = 0			-5			-5		
loff		VCC = 0, VI or VO = 0 to	1.5 V	A 1 Is	Negative and a		Personal Property	na managa	±100	μА	
(-25 1191 (-1 1191		V- OV	V _I = 0.8 V	75	· energy in a		75			. A	
I(hold)	A inputs	VCC = 3 V	V _I = 2 V	-75	Y		-75			μА	
lozh		V _{CC} = 3.6 V,	V _O = 3 V		-	- 1		particular state	1	μА	
lozL		V _{CC} = 3.6 V,	V _O = 0.5 V		Y	-1	- 3		-1	μА	
lozpu	5.6	$\frac{V_{CC}}{OE} = 0 \text{ to } 1.5 \text{ V}, V_{O} = 0.$	5 V to 3 V,			±100*		0	±100	μΑ	
lozpd	9,8	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = 0.$	5 V to 3 V,			±100*			±100	μА	
	6.8	8 8 88	Outputs high	01		0.19			0.19	591	
Icc		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs low	1 27	-	5	-		5	mA	
		Al = ACC of GIAD	Outputs disabled	8 5		0.19			0.19		
∆lcc [‡]		V _{CC} = 3 V to 3.6 V, One ii Other inputs at V _{CC} or GN	nput at V _{CC} – 0.6 V,		OVE	0.2	0.8 mm	V to one	0.2	mA	
0	Control inputs	V 0V-0	ig to the dame alrection	distance of	3.5	he same	to alugh	3.5	na meby	dd wal	
Ci	Data inputs	V _I = 3 V or 0			4.5			4.5		pF	
Co		V _O = 3 V or 0			11		N TOTAL P	11		pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. † This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTH16835, SN74LVTH16835 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	ecsathtv.ia	THI GBOS. SNI	SNSALV	5	SN54LV7	TH16835		5	SN74LV	TH16835		
					V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		3.3 V 3 V	V _{CC} = 2.7 V		UNIT
					MAX	MIN MA	MAX	MIN	MAX	MIN	MAX	>nV
fclock	Clock frequency		5.0	Arms	150	THE STATE OF	150	Law e	150		150	MHz
, V	Dulas division	LE high				3.3		3.3		3.3		HOY
t _W	Pulse duration	CLK high or low				3.3		3.3	VCC =	3.3		ns
	0.0	Data before CLK1		1.6	45	2.1		1.6		2.1		
tsu	Setup time	Data bafasa I.E.I.	CLK high	2.6	100	1.9		2.6	= 00V	1.9	14-1	ns
		Data before LE↓	CLK low	2		1.3		2		1.3		
V	Data days	Data after CLK↑		2	03	2.1		2		2.1		ns
th	Hold time	Data after LE↓	a after LE↓			1.2	1.2		0.9		1.2	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

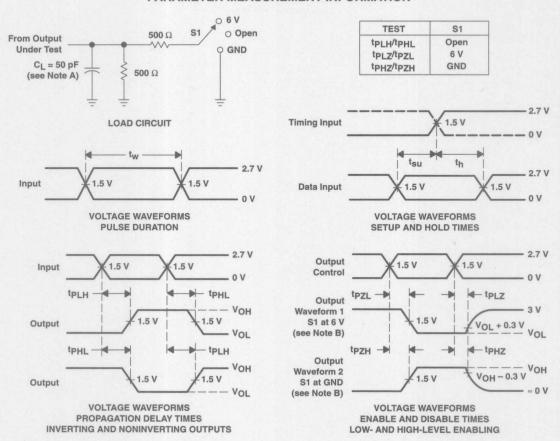
Aut I			9	SN54LV	TH16835			SN74	LVTH16	835			
PARAMETER	FROM (INPUT)		TO (OUTPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			2.7 V	UNIT
-5			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
fmax			150		150		150		44.	150		MHz	
tPLH	A	Y	1.7	5.4		6.8	1.7	3	5.4	1- 2	6.8	(blod)	
tPHL	A		1.6	5.9		7.7	1.6	3.2	5.9		7.7	ns	
tPLH	LE	Y	2.3	7		8.5	2.3	4	7		8.5	7730	
tPHL	LE		2.7	7.9		9.7	2.7	4.3	7.9		9.7	ns	
tPLH	01.14	100 ta	2.5	7.9		9.2	2.5	4.1	7.9		9.2	ns	
tPHL	CLK	1	3.5	8.9	V.A.	10.4	3.5	5.4	8.9		10.4	ns	
^t PZH		Y	1.2	5		5.9	1.2	3	5		5.9	8420	
tPZL	ŌĒ	ler.o	1.5	5.8	anighiO	6.9	1.5	3	5.8		6.9	ns	
tPHZ		Y	2.7	7.4	afudluQ	8.3	2.7	4.6	7.4		8.3	ns	
tPLZ	ŌĒ	OE Y	2.8	6.7	eingtu	7.2	2.8	4.7	6.7		7.2	ns	
tsk(o) [‡]				Ve	- auv	is luqui i	go V a	E at V 8	0.5			ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] Skew between any two outputs of the same package switching in the same direction

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

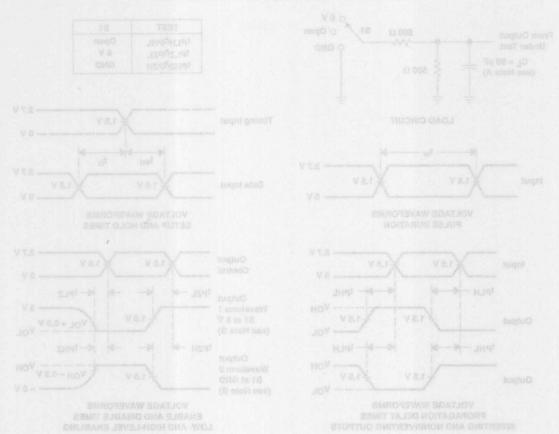


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz. Z_O = 50 Ω, t_r ≤ 2.5 ns. t_r ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- VOTES: A. O. Includes probe and ill oppositance.
- Waveform 1 is for an output with internal conditions such that the output is ligh except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output aparticle.
- All trout pulses are auxobed by ownershots having the following characteristics: PER < 10 MHz: Zo = 50.0, 1, < 2.5 oz. (x < 2.5 oz. (x
 - The outputs are measured one at a time with one transition por measurement.

Figure 1, Load Circuit and Voltage Waveforms



SN54LVTH16952, SN74LVTH16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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•	Members of the Texas Instruments Widebus™ Family		SN74LVTH16952		WD PACKAGE GG OR DL PACKAGE
stor;	State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation		1OEAB [1 2 3	56] 1OEBA 55] 1CLKBA 54] 1CLKENBA
•	Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V _{CC})			4	53 GND 52 1B1
•	Support Unregulated Battery Operation Down to 2.7 V		00 .	6 7	51 1B2 50 V _{CC}
•	High-Impedance State During Power Up and Power Down		1A4 [8 9	49 1B3 48 1B4
•	Typical V _{OLP} (Output Ground Bounce) < 0.8 V at V _{CC} = 3.3 V, T _A = 25°C		1A5 [GND [1A6 [11	47] 1B5 46] GND 45] 1B6
•	Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors			13 14	44 1 1B7 43 1 1B8 42 1 2B1
•	Power Off Disables Outputs, Permitting Live Insertion		2A2 [16	41 2B2 40 2B3
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise		GND [2A4 [39 GND 38 2B4
•	Flow-Through Architecture Optimizes PCB Layout		2A5 [2A6 [21	37 2B5 36 2B6
•	Latch-Up Performance Exceeds 500 mA Per JESD 17		2A7 [22	35 V _{CC} 34 2B7
•	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)		2A8 [GND [2CLKENAB [2CLKAB]	25 26	33 288 32 GND 31 2CLKENBA 30 2CLKBA
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings			28	29 2OEBA

description

The 'LVTH16952 devices are 16-bit registered transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.



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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16952 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16952 is characterized for operation from –40°C to 85°C.

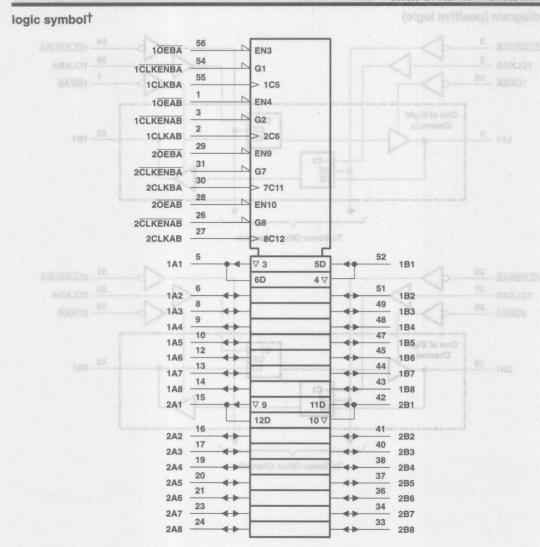
FUNCTION TABLET

aV	INPUTS								
CLKENAB	CLKAB	OEAB	A	В					
Al H	X	L	X	B ₀ ‡					
X	L	L	X	B ₀ ‡					
MOL	1	L	L	Load					
Al L	1	L	H	H.					
X	X	Н	X	Z					

† A-to-B data flow is shown; B-to-A data flow is similar, but uses CLKENBA. CLKBA, and OEBA.

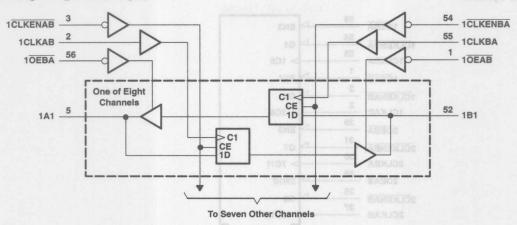
‡Level of B before the indicated steady-state input conditions were established

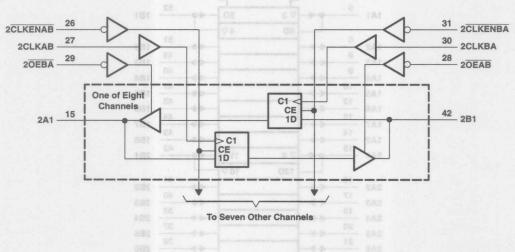
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[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN54LVTH16952, SN74LVTH16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state, Vo (see Note 1)	
Current into any output in the low state, Io: SN54LVTH16952	
SN74LVTH16952	
Current into any output in the high state, Io (see Note 2): SN54LVTH16952	. 90 48 mA
SN74LVTH16952	64 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, IOK (VO < 0)	–50 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	
DL package 17	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		7.5	V 8.0 a JV	SN54LVT	H16952	SN74LVT	H16952	
				MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		.V & at V 8.0	QV 2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage			2	3 (1000 = 3	2		٧
VIL	Low-level input voltage		.V € 01 V 8.0 ±	OA 'n ou A	0.8	W I	0.8	V
VI	Input voltage	· · · · · · · · · · · · · · · · · · ·		Comment in comment	5.5		5.5	٧
ЮН	High-level output current	ar ar ar ar a	Tight diament	N. N.	-24	N.	-32	mA
loL	Low-level output current			GMO s	48		64	mA
Δt/Δν	Input transition rise or fall rate		Outputs enabled		10		10	ns/V
Δt/ΔVCC	Power-up ramp rate		CHE)	200	duction tier	200		μs/V
TA	Operating free-air temperature			-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54LVTH16952, SN74LVTH16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS697D - JULY 1997 - REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

15.00		7507.0	CHRITICHIC	SN54LVTH1	6952	SN74LVTH16	952	UNIT
PAI	RAMETER	IESI C	CONDITIONS	MIN TYPT	MAX	MIN TYPT	MAX	UNIT
VIK	-0.5	V _{CC} = 2.7 V,	I _I = -18 mA	(f stok	-1.2	V .etale No-16	-1.2	V
4 0.6 \	-0.5 V to Vac	V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.2	eny or	V _{CC} -0.2	sage re	Vol
m 89		V _{CC} = 2.7 V,	IOH = -8 mA	2.4	ol ant ni	2.4	ni Inen	VCu
VOH		V 0.V	I _{OH} = -24 mA	2				V
		VCC = 3 V Sagari	I _{OH} = -32 mA	igh ergine to la	n am n	2	ni men	
um dä-		V 07V	I _{OL} = 100 μA		0.2	1 4	0.2	es est
		V _{CC} = 2.7 V	I _{OL} = 24 mA	100	0.5	I tagawan man	0.5	
			I _{OL} = 16 mA	La Ison Note 3	0.4	neomi lacced	0.4	V
VOL		V 2V	I _{OL} = 32 mA		0.5		0.5	V
		VCC = 3 V	I _{OL} = 48 mA	· ·	0.55	imperature ra	et egist	
		and Transition of the same	I _{OL} = 64 mA	"sourcides anaméricas a	thingsis."	ingen Ustridu under	0.55	
on al "en	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	tstunco sertio yea s	= ±1	on of the device	±1	enottor
	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	ed conditions for er	10	enm-eluloschi cit i	10	
lj Joen	A MARCO ON SERVINO	Michiga de Cara de	V _I = 5.5 V	in sideni zi tuctuo a	20	don awall triansus	20	μΑ
	A or B ports‡	V _{CC} = 3.6 V	VI = VCC	e la celculated in a	nabaq 1 n	lamnarit agaileac	eriT 1	
	1		V _I = 0		-5		-5	
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V	M ees suon	ibnos	gnustedo o	±100	μΑ
learner a	A or B ports	STEATON	V _I = 0.8 V	75		75		
II(hold)	A or B ports	VCC = 3 V	V _I = 2 V	-75		-75		μА
lozpu	2.7 3.6	$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	= 0.5 V to 3 V,		±100*	egatlov vic	±100	μА
IOZPD	8.0	$\frac{V_{CC}}{OE} = 1.5 \text{ V to 0, V}_{O} = \frac{V_{CC}}{OE} = \frac{1.5 \text{ V to 0, V}_{O}}{OE} = 1.$	= 0.5 V to 3 V,		±100*	gallov tuqrii feval	±100	μА
	\$6-	V _{CC} = 3.6 V,	Outputs high		0.19	-	0.19	-
lcc		10 = 0,	Outputs low		5		5	mA
AUI	94(3	V _I = V _{CC} or GND	Outputs disabled		0.19		0.19	
ΔICC§	200	V _{CC} = 3 V to 3.6 V, Or Other inputs at V _{CC} or	ne input at V _{CC} - 0.6 V, GND		0.2	er-up ramp rete	0.2	mA
Ci	60- 10-	V _I = 3 V or 0		4	a manad	4	000	pF
Cio	racedqual Fentor	V _O = 3 V or 0	added exinstrator days to 00).	10	HAR CBALL	10	ATT UNUSE	pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ Unused pins at V_{CC} or GND

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVTH16952, SN74LVTH16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

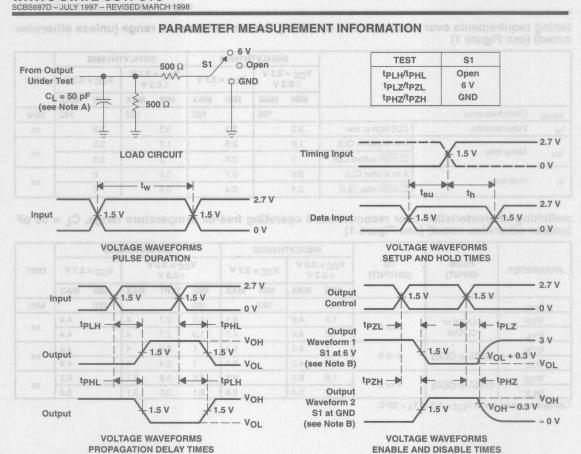
		TEST		SN54LVTH16952			5	SN74LV	TH16952		
				3.3 V 3 V	Vcc=	2.7 V	V _{CC} =		Vcc=	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	0
fclock	Clock frequency			150		150		150		150	MHz
t _W	Pulse duration	CLK high or low	3.3		3.3		3.3	1	3.3		ns
V 7.2		A or B before CLK	1.9		2.5		1.7		2.5		
t _{su}	Setup time	CLKEN before CLK	2		2.8	F3 1	2	U UAQ.	2.8		ns
	Hald time	A or B after CLK			0.7		0.8		0		
th	Hold time	CLKEN after CLK	0.4		0.4	0.4		M	0		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

	SKIRIOPEIKS		SN54LVTH16952				SN74LVTH16952					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V	V _{CC} = 2.7 V		UNIT
	WAY .		MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
fmax			150		150	0	150			150	and a second	MHz
tPLH	CLKBA or	A or B	1.3	4.6		5.1	1.3	2.7	4	- W. 10	4.4	ns
tPHL	CLKAB	AOLP	1.3	4.6		4.7	1.3	2.7	4		4.4	115
tPZH	OFDA - OFAD	A or B	1	4.3	210	5.1	1/1	2.3	4		4.9	
tPZL	OEBA or OEAB	AOIB	1.2	4.2	30	5.1	1 1	2.4	4	-	4.9	ns
tPHZ		A or B	1.8	6.2		6.5	2.1	3.9	5.7	Be 86	6.2	
tPLZ	OEBA or OEAB	BA or OEAB A or B		5.4		5.6	2.1	3.5	5.1		5.3	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.





NOTES: A. CL includes probe and jig capacitance.

INVERTING AND NONINVERTING OUTPUTS

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$,

LOW- AND HIGH-LEVEL ENABLING

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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Low-Cost, Low-Power Level Shifting in Mixed-Voltage Systems

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Introduction

The increasing demand for lower system power consumption has brought many new design challenges. Among them is the problem of safely and efficiently interfacing the various switching levels in today's mixed 3.3-V and 5-V systems while maintaining the lowest possible total system power consumption. Two competing methods of accomplishing this mixed-mode signal translation have emerged:

- Split-rail or dual 3.3-V and 5-V VCC devices
- Completely 5-V tolerant, pure 3.3-V V_{CC} components

This application report deals with the pros and cons of using both device types and offers additional suggestions for even greater system power savings.

Split-Rail Level Shifters and the service and

Split-rail level shifters are a class of transceiver devices that have both a 5-V and 3.3-V V_{CC} rail. Products in this class can be used effectively as level shifters and datapath voltage translators, but the following precautions are usually recommended:

- Dual-V_{CC} rail devices typically have strict power sequencing requirements to prevent leakage or even damage to
 the devices in the event that one V_{CC} rail ramps faster than the other. These stringent requirements are often difficult
 to meet from a system-timing standpoint and offer little flexibility for partial system power down or other advanced
 power-saving design techniques.
- Simply because the device has a 5-V V_{CC} pin does not necessarily ensure that the part will actually switch all the
 way to the 5-V rail. Switching to 5 V is one way to reduce the power consumption in 5-V memories or other pure
 5-V CMOS circuits that are driven by a level-shifter device (this application report will demonstrate others as well).

The data sheet for the product in question reveals whether the part drives all the way to the 5-V rail. If the output high-voltage (V_{OH}) minimum is around 4.44 V, it does drive to the rail. Five-volt level shifters with TTL-compatible outputs typically drive only to around 3.6 V.

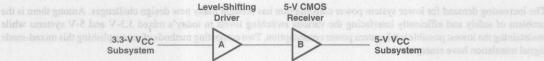
5-V Tolerant, Pure 3.3-V V_{CC} Level Shifters

A second class of products created to meet these design challenges offers the same voltage translation and level-shifting capabilities as the split-rail devices previously mentioned. From a single V_{CC} source, they avoid the power-sequencing problems of the split rails and also are offered in a number of functions, bit widths, and storage options. The one potential drawback of the single- V_{CC} products is that the outputs do not pull all the way to the 5-V V_{CC} rail. But, is this really a drawback?

The Misconception About △ICC

The component selection of a level shifter impacts two major aspects of total system-power dissipation:

- The impact that the V_{OH} level of the driving part (A, in Figure 1) has on the power dissipation of the receiving device (B, in Figure 1), commonly known as ΔI_{CC}
- The power of the device itself



Note: Unidirectional mode illustrated for simplicity.

Figure 1. Basic Logic Data Transceiver

 ΔI_{CC} is the added power dissipation induced into a TTL-compatible 5-V CMOS device (B, in Figure 1) due to the V_{OH} level of the driving device (A, in Figure 1). It would be correct to expect that a TTL-compatible 5-V CMOS product have higher power dissipation if it was driven by a device with a V_{OH} of 3.6 V than if that same device was driven by a 5-V V_{OH} driver.

Figure 2 shows a typical CMOS input stage and the ΔI_{CC} current associated with switching the device through the input voltage range from 0 to V_{CC} .

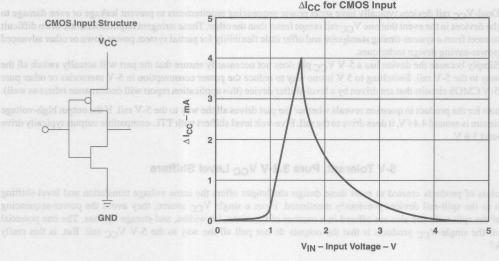


Figure 2. Basic CMOS Input Structure and Typical △I_{CC} Current

As expected, the ΔI_{CC} current approaches zero at the V_{CC} and ground rails, and peaks in the TTL-threshold region of 1.5 V. Figure 3 is a graph of the ΔI_{CC} (i.e., additional I_{CC}) that is induced into a 16-bit device (all outputs switching) as a function of V_{OH} and frequency.

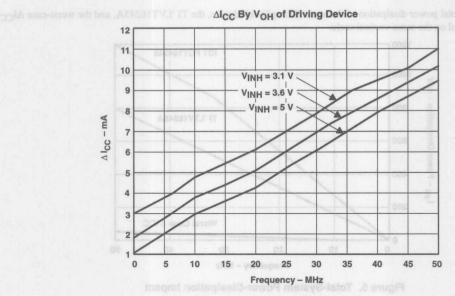


Figure 3. ΔI_{CC} - 16-Bit Device

As shown in Figure 3, ΔI_{CC} is, in fact, 2 to 3 mA higher for the case where V_{OH} is only 3.1 V, than for the same device driven to the 5-V rail by a pure 5-V CMOS device. From this, one might conclude that the best possible solution would be to always select a part that switches all the way to the 5-V rail, but this conclusion fails to consider the impact of system power on the driving device.

Figure 4 shows the V_{OH} of two devices: the FCT164245 split-rail device from Integrated Device Technologies (IDT) and the LVT16245A from Texas Instruments.

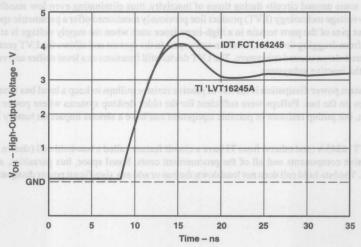


Figure 4. VOH of FCT164245 and 'LVT16245A

From Figure 4, it can be correctly concluded that the induced ΔI_{CC} current in a part driven by the LVT part would be higher than the FCT device. The problem with this conclusion is that ΔI_{CC} is only one of the two components of total system power dissipation that selection of a level-shifter device has from a system standpoint.

Figure 5 shows the total power dissipation of the same IDT split-rail device, the TI 'LVT16245A, and the worst-case ΔI_{CC} ($V_{OH} = 3.1~V$) plotted on the same vertical scale.

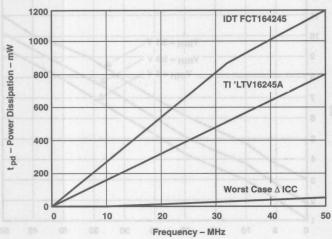


Figure 5. Total-System Power-Dissipation Impact

From Figure 5, it can be seen that, even if a split-rail device pulls all the way to the 5-V rail (which the IDT part does not), the power savings in ΔI_{CC} is more than offset by the huge switching currents that the split rail draws from the 5-V rail. The negative implications on heating, reliability, and battery life are obvious.

More Savings Are Possible

Some systems use a means of power savings known as partial power down. In partial power-down mode, a system basically shuts off the V_{CC} to some unused circuits during times of inactivity, thus eliminating even low standby currents. All of the members of TI's low-voltage technology (LVT) product line previously mentioned offer a parametric specification I_{off} , which ensures that the output pins of the parts remain in a high-impedance state when the supply voltage is at 0 V. This prevents an inactive LVT device from dragging down the bus of an active part in the system and allows the LVT part to become a partition for the partially powered-down unused subsystem. The LVT device still functions as a level shifter and voltage translator when power is restored to the inactive subsystem.

Another aspect of system power dissipation is the use of passive resistor pullups to keep a local bus from floating and causing damage to the devices on the bus. Pullups were sufficient for the older desktop systems where power consumption was not as much of a concern, but pullup resistors in portable equipment can have a serious impact on battery life, and as such must be addressed.

Products like the 'LVT16245A (and others) from TI have a circuit feature called a bus-hold cell (shown in Figure 6). This cell eliminates these passive components and all of the procurement costs, board space, bus parasitics, and power dissipation associated with them. The bus-hold cell does not load down the bus or add any significant power dissipation to the LVT device.

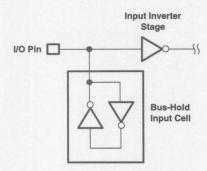


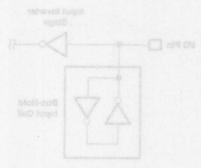
Figure 6. LVT Bus-Hold Cell

Conclusion

Mixed 3.3-V and 5-V systems can be optimized for low power and low cost by the judicious selection of the appropriate voltage-level shifter component. Split-rail level shifters can affect this voltage translation, but selection of this device is burdened with serious design tradeoffs in power sequencing, partial system power down, and system power dissipation. Further savings in both power and component cost can be realized if the component selected has a bus-hold cell or other means of eliminating passive system components.

Acknowledgment

The author of this document is Mark McClear:



Agure 6, LVT Bus-Hold Cell

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Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices

SCZA005B March 1998



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Thermal Considerations for Standard Linear and Logic (SLL) Packages and Devices

Users of Texas Instruments (TI™) SLL products must consider device power dissipation, package power capability, and maximum ambient temperatures when designing with these products. The product users also need to be aware of the long-term reliability impact of maximum device-junction temperatures.

This application report is intended to help users understand and evaluate these factors. Three concepts — package thermal performance, device power dissipation, and reliability — are discussed in separate sections.

The first section, $Package\ Thermal\ Performance$, includes data about the recently developed EIA/JEDEC Standard JESD 51 for package thermal-impedance measurement. It discusses most SLL package types and lists θ_{JA} (thermal impedance) values for those packages.

The second section, *Power Calculation*, discusses the power consumption by CMOS and BiCMOS/bipolar semiconductors. Standard formulas are given that allow the user to calculate the maximum power dissipated by a device in a typical application using data-book specifications, operating frequency, and voltage. The only characteristic not readily known is the output loading of the devices under consideration.

The third section, Benefits of Minimizing Power Consumption, discusses ways to reduce power consumption and the benefits thereof.

The final section, *Reliability Implications*, discusses the effects of chip temperature on reliability and electromigration. Information presented in this section allows the user to make an informed judgment as to the maximum chip temperature versus device wearout acceptable in the particular application.

The recommended analysis procedure is to assume a maximum chip temperature (see *Reliability Implications*) then, using θ_{JA} values for the chosen package (see *Package Thermal Performance*) and the known environmental requirements, calculate the maximum permissible power for that package. The formula presented in the *Power Calculation* section can then be used to ensure the operating conditions do not exceed the power capability of the chosen package type. Of course, the user can choose to calculate the maximum power from the application, then select a package that can meet the power dissipation requirement.

Bieven St. L. packages were tested using a JEDEC test-board design and commend to Therms AL model results to validate the

Package Thermal Performance

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{1A} = \frac{T_j - T_a}{R} \tag{1}$$

Where:

 T_i = chip junction temperature

 $T_a = ambient temperature$

P = device power dissipation

 θ_{JA} values are also the most subject to interpretation. Factors that can greatly influence the measurement and calculation of θ_{JA} are:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

JEDEC established the JC 15.1 committee, comprising industry representatives, to develop industry-standard specifications for thermal testing. The specifications include development of electrical test procedures, careful descriptions of appropriate test environments, guidelines for the design of thermal test chips, guidelines for thermal modeling, and specifications for component mounting. The specifications for component mounting are divided into a series for different package types. The specifications include test-board descriptions for low effective thermal-conductivity test boards with a single metal layer and high effective thermal-conductivity test boards with embedded solid copper planes simulating system power and ground planes.

In August 1996, the Electronics Industries Association released JESD 51-3 titled Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages. The standard describes guidelines with parameters for thermal-test-board design for low effective thermal conductivity (one signal layer in the trace fanout area) as differentiated from a multilayer printed-circuit board (PCB), which might include power and ground planes. The specified parameters include the area of the test board, the amount of copper traces on the test board, and the resulting trace fanout area, each important to the heat-sinking characteristics of the PCB. Prior to release of the standard, thermal-impedance data for similar packages varied widely within the industry due to the use of different test-board designs. As the industry adopts this standard methodology, thermal-impedance variations from test-board design should be minimized.

Key features of the standard test-board design are:

- Board thickness: 0.062 in.
- Board dimensions: 4.0 × 4.5 in. for packages > than 27 mm in length, 3.0 × 4.5 in. for packages ≤ 27 mm in length
- Trace thickness: 0.0028 in.
- Trace length: 25.0 mm (0.984 in.)

The SLL product group uses test boards designed to JESD 51-3 for thermal-impedance measurements. The parameters outlined in the standard also are used to set up thermal models. The thermal-model program used by SLL is ThermCAL, a finite-difference thermal-modeling tool.

Eleven SLL packages were tested using a JEDEC test-board design and compared to ThermCAL model results to validate the correlation between model results and data (see Table 1). This comparison shows that the models are accurate to within 10% of measured data. In many cases the model data varies from measured data by less than 5%.

Table 1. Package Comparison

MODELED MODELED	PACKAGE TYPE (PINS, DESIGNATION)	DIE SIZE (mils)	θJA MEASURED (°C/W)	θJA MODELED (°C/W)	CHANGE (%)		
	56 DL	120 × 120	73.5	78.3	6.5		
	20 DW	62 × 62	96.6	90.9	-5.9		
	160 PCM	240 × 240	34.9	34.9	0	d	
	52 PAH [†]	120 × 120	87.2	92.2	5.7	wei	
	52 PAH [‡]	120 × 120	72.7	75.2	3.4	Wd	
	100 PZ	360 × 360	45	42.8	-4.9	Wa	
	208 PDV	240 × 240	50.1	52.8	5.4	-	
	48 DGG	120 × 120	89.1	93.5	4.9	BCI	
	14 DGV	62 × 62	181.5	191.7	5.6	80	
	48 DGV	62×186	92.9	89.9	-3.2	80	
	100 PCA	240 × 240	33.3	34.9	4.8	80	
	† S-pad leadframe	: 78 118.	10 61	× 80	NS-137	gad	

F Conventional leadframe

After the accuracy of the model results was established, all other SLL packages could be modeled. θ_{IA} data based on JESD 51-3 is available for all SLL leaded surface-mount packages (see Table 2). The data is grouped by package type with values of θ_{IA} shown at different airflow levels. Leadframe pad size and die size are shown.

Junction-to-case thermal-impedance (θ_{IC}) data is shown with the junction-to-ambient data. Measured θ_{IC} data was generated for the packages tested using the JEDEC PCB. Previously published values of θ_{JC} are used for packages not yet tested using the PCB designed to JESD 51-3.

Table 2. SLL Package Thermal-Impedance Data

PIN	TI PACKAGE	JEDEC	PAD SIZE	CHIP SIZE (mils)	θJA (°C/W) AT AIRFLOW (LFM)				MEASURED/	θјС
COUNT		SPECIFICATION	(mils)		0	150	250	500	MODELED	(°C/W)
		E. E.O.	183 TT 184	SOIC	USA		ACL OF	-		
14	D	MS-012	70×70	32×37	126.6	104	96.4	87.4	Modeled	46
16	D	MS-012	90×90	44×65	112.6	91.2	83.9	74.8	Modeled	42
20	DW	MS-013	90×110	62 × 62	96.6	82.2	77.7	71.5	Measured	38.3
24	DW	MS-013	140×160	84 × 122	80.7	53.7	47.5	40.7	Modeled	25
28	DW	MS-013	120×140	90 × 128	78.2	54.3	48.4	41.9	Modeled	
		4.6	13E	SSOP	(SIQ	Y4	74 805			
14	DB	MO-150	71×71	43 × 52	158	128.6	118.9	106.5	Modeled	47
16	DB	MO-150	83×91	51×61	130.8	105.9	97.3	86.5	Modeled	47
20	DB	MO-150	87×106	61 × 65	114.6	92	84	74.7	Modeled	45
24	DB	MO-150	87×106	74×91	104.2	83.5	76.3	67.5	Modeled	42
20	DBQ	MS-137	96×140	61×75	118.1	95.3	86.9	76.7	Modeled	46
24	DBQ	MS-137	96×140	61 × 75	113	92	84.1	74.6	Modeled	42
28	DL	MO-118	150×180	97 × 142	97	77.2	70.9	63.1	Modeled	2011
48	DL	MO-118	120×180	73 × 128	93.5	69.9	63.8	57.1	Modeled	26
56	DL	MO-118	150 × 220	120 × 120	73.5	62.3	59	54.6	Measured	27.3
emetare)	JC data was g	n data. Messamed B	ocnon-to-ambie	PLCC	in alread	misp ()	(B) 300s	mpedi	James Dennal	1-0083
28	FN	MS-018	300 × 348	214×319	70.9	58.8	52.7	46	Modeled	26.7
44	FN	MS-018	270×270	235 × 235	46.2	38.6	35.4	31.6	Modeled	22
68	FN	MS-018	325 × 325	280 × 280	39.3	33	30.5	27.6	Modeled	14.5
84	FN	MS-018	275 × 275	188 × 185	39.7	33.9	31.8	29.4	Modeled	11.9
				QFP						
52	RC	MS-022	210 × 210	120 × 120	78.9	48.4	43.6	38.1	Modeled	20
80	PH		265 × 265	232 × 240	76.1	67.9	61.4	53.6	Modeled	15.1
132	PQ	MO-069	315×315	272 × 272	46.3	34.5	31.6	28.3	Modeled	9.8
144	PCM	MS-022	433 × 433	338 × 338	38.8	27.3	25.1	22.4	Modeled	14.5
160	PCM	MS-022	511 × 511	433 × 433	34.9	29.9	28.3	24.7	Measured	11.4
208	PPM	MO-143	413 × 413	268 × 268	36.7	30.4	28.1	26.7	Modeled	
				TQFP					h de la compa	
52	PAH	MO-136	S-Pad	120 × 120	87.2	76.1	71.5	67	Measured	28.3
52	PAH	MO-136	3.5 × 3.5 mm	120 × 120	72.7	62.6	59.2	53.8	Measured	24.0
64	PM	MO-136	6.75 × 6.75 mm	235 × 235	66.9	53.6	47.6	40.6	Modeled	10.4
64	PAG	MO-136	S-Pad	240 × 240	58.2	48.8	45.2	40.3	Measured	22.6
80	PN	MO-136	S-Pad	240 × 240	61.5	52.8	49.3	44.6	Measured	26.4
100	PZ	MO-136	S-Pad	360 × 360	45	38.3	35.3	27.9	Measured	7.6
100	PZ	MO-136	S-Pad	240 × 240	50.1	42.7	40.4	36.8	Measured	21.1
100	PCA	MO-136	6.5 × 6.5 mm	240 × 240	33.3	24.7	21.8	19.2	Measured	4.3
120	PCB	MO-136	6.5 × 6.5 mm	240 × 240	28.1	22.3	21	18	Modeled	3.3
144	PGE	MO-136	342 × 350	378 × 378	48.3	39.1	35.5	31	Modeled	9.9
208	PDV	MO-136	S-Pad	240 × 240	50.1	43.63	40.9	37.3	Measured	9.9

Table 2. SLL Package Thermal-Impedance Data (Continued)

PIN	TI	JEDEC SPECIFICATION	PAD SIZE	CHIP SIZE	θЈА	(°C/W) A (LF		Low	MEASURED/ MODELED	θJC (°C/W)
COUNT	PACKAGE	SPECIFICATION	(mils)	(mils)	0	150	250	500	MODELED	(C/W)
fTT in na	ils, when driv	sad BIOMOS ince	aneauble CMOS	SOP	dam sh	subivit	n Uncip	feend	e values can be	an'il a
14	NS	EIAJ-TYPE-II	79 × 87	55 × 57	127.1	103.7	95.5	85.2	Modeled	95
16	NS	EIAJ-TYPE-II	87 × 142	76×86	111.3	89.3	81.4	71.5	Modeled	95
20	NS	EIAJ-TYPE-II	87×118	60×77	100.3	82.8	76.2	68	Modeled	90
fogua-19	woo enimate	lons are made to de	L Power enlanta	TSSOP	d Jaums	msod a	no solv	ab ribiga	not notigmore	000750481
14	PW	MO-153	71×71	48 × 53	169.8	146.7	136	121.7	Modeled	35
16	PW	MO-153	104 × 104	56×76	148.9	127.9	117.6	103.9	Modeled	35
20	PW	MO-153	102×106	53 × 69	128	110.6	101.9	90.8	Modeled	34
24	PW	MO-153	94 × 140	74×91	119.9	98.8	90.6	80	Modeled	33
48	DGG	MO-153	4.6 × 3.2 mm	120 × 120	89.1	78.5	75.1	69.4	Measured	25.2
56	DGG	MO-153	3.94 × 5.08 mm	132 × 176	81.2	72.8	65.8	57.9	Modeled	13
64	DGG	MO-153	5.7 × 3.6 mm	120 × 120	72.9	63.3	61.8	57.1	Measured	21.3
Cempinens.	to Storen neur	WHICH STREET IN CHILD	ED DED UT DESIGN	TVSOP	y ar dom	anusqa.	OUTERS	all sork	on consideration	DISH NAME OF STREET
14	DGV	MO-194	75×75	62 × 62	181.5	165.8	159.5	150.4	Measured	66.7
16	DGV	MO-194	75×75	65 × 65	179.6	153.2	141.7	126.3	Modeled	
20	DGV	MO-194	104 × 104	94×94	146.1	122.3	111.6	97.4	Modeled	
24	DGV	MO-194	104 × 104	94 × 94	138.6	116.2	106.2	93.2	Modeled	
48	DGV	MO-194	100 × 240	62×186	92.9	80.9	77.1	71	Measured	27.2
56	DGV	MO-194	100×274	90×262	85.9	64.6	57.1	48.4	Modeled	slever
80	DBB	MO-194	100 × 224	93 × 203	105.6	78.4	71.8	63.7	Modeled	vices.
			PDIP (assur	nes zero trace	length)			, ni	73	
8	P	MS-001			104			rv o	hagans at D.	41
14/16	N	MS-001			78	(5 V)	hay =	laval a	nol dald = 1	32
20	N	MS-001			67	(V 0) b	nozz =	level o	golwol = 0	33
24	NT	MS-001			67	Trwe Jo.	D, leut 3	to I an	io i'aob = X	25
		BGA		amgiri pe) (slik)	(i) balo	moun	у суси	UD 8800 = D	
256	GFN	MO-151	eas) perod radure	EREIQ-RO-ING	42	DIST LA) andtin	A chest	ANAM data	6.2
388	GFW	MO-151			18.9	sd mr	201 Mg	STATUTE LOSS	Model data	

sing equations expaning a mine routowing accurate, which the LCC versus frequency of alternation (see Figures 2 and 3). The slope of the curve provides a value in the formulaplied by the number of outputs switching and the desired frequency, provides the dyna

Power Calculation

Reduction of power consumption makes a device more robust and reliable. When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account. Both bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output (I_{CCL} , I_{CCH} , or I_{CCZ}), while a CMOS device has a single value for I_{CC} . These values can be found in the individual data sheets. TTL-compatible CMOS and BiCMOS inputs, when driven at TTL levels, also consume additional current because they may not be driven all the way to V_{CC} or GND; therefore, the input transistors are not switched completely off. This value, known as ΔI_{CC} , also is provided in the data sheet.

Due to the high operating frequencies, there is a strict limit on power consumption in computer systems. Therefore, allowable power consumption for each device on a board must be minimized. Power calculations are made to determine power-supply sizing, current requirements, cooling/heatsink requirements, and criteria for device selection. Power calculation also can determine the maximum reliable operating frequency.

There are two components that establish the amount of power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

Dynamic power consumption results from charging and discharging external load and internal parasitic capacitances. The parameter for CMOS device parasitic capacitance is C_{pd} , which is listed in the data sheet and is obtained using equations 2 and 3:

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_{I}} - C_{L(eff)}$$
 (2)

$$C_{L(eff)} = C_L \times N_{SW} \times \frac{f_0}{f_1}$$
(3)

To explain the C_{pd} and the method of calculating dynamic power, see Table 3, which indicates the C_{pd} test conditions for AHC devices. The symbols used in Table 3 are:

$$V = V_{CC} (5 V)$$

G = ground(0 V)

1 = high logic level = V_{CC} (5 V)

0 = low logic level = ground (0 V)

X = don't care: 1 or 0, but not switching

C = 50% duty cycle input pulse (1 MHz) (see Figure 1)

D = 50% duty cycle input (1/2 frequency) out-of-phase input pulse (see Figure 1)

S = standard ac output load (50 pF to GND)

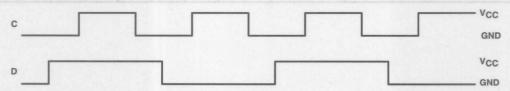


Figure 1. Input Waveform

Table 3 shows the switching of each pin for AHC devices. Once the C_{pd} is determined from the table, the P_D is easy to calculate using equations explained in the following sections.

Although a C_{pd} value is not provided for ABT and LVT, the I_{CC} versus frequency curves display essentially the same information (see Figures 2 and 3). The slope of the curve provides a value in the form of mA/(MHz × bit), which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device without the load current. Equations 4 through 14 can be used to calculate total power for CMOS or BiCMOS devices.

Table 3. C_{pd} Test Conditions With One- or Multiple-Bit Switching

								PIN NO.												
TYPE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AHC00	С	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC02	S	C	0	S	X	X	G	X	X	S	X	X	S	V						
AHC04	C.	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC08	C	1	S	X	X	S	G	S	X	X	S	X	X	V						1
AHC10	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC11	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC14	C	S	X	S	X	S	G	S	X	S	X	S	X	V					F	
AHC32	C	1	S	X	X	S	G	S	X	X	S	X	X	V				-		
AHC74	1	D	C	1	S	S	G	S	S	X	X	X	1	V	236	The sale	Distance of the last of the la			
AHC86	C	1	S	X	X	S	G	S	X	X	S	X	X	V		1	Table.			
AHC138	C	0	0	0	0	1	S	G	S	S	S	S	S	S	S	V		32+0		
AHC139	0	С	0	S	S	S	S	G	S	S	S	S	X	X	X	V		15		
AHC240	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC244	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC245	1	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC373†	0	S	D	D	S	S	D	D	S	G	С	S	D	D	S	S	D	D	S	V
AHC374 [‡]	0	S	D	D	S	S	D	D	S	G	С	S	D	D	S	S	D	D	S	V
AHC540	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC541	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC573†	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V
AHC574‡	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V

† All bits switching, but with no active clock signal ‡ All bits switching

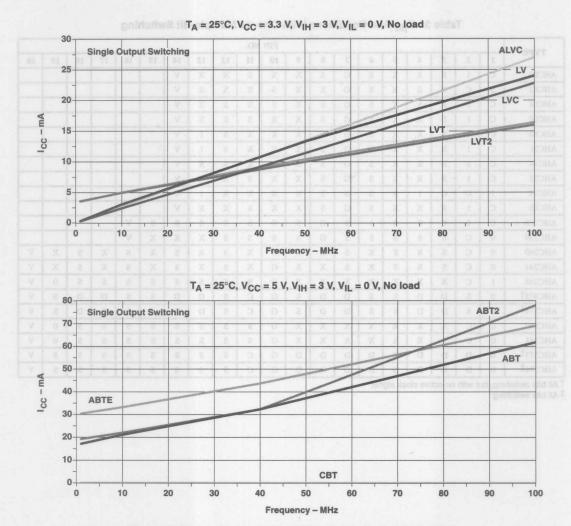
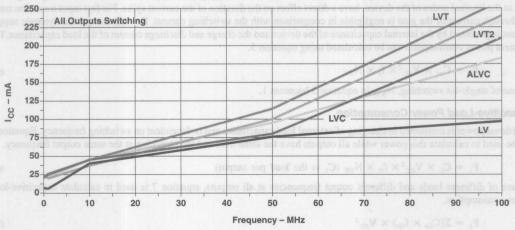


Figure 2. Power Consumption With a Single Output Switching





TA = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, No load

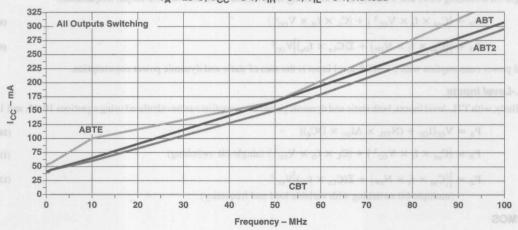


Figure 3. Power Consumption With All Outputs Switching

CMOS

CMOS-Level Inputs

Static power consumption can be calculated using equation 4.

$$P_{S} = V_{CC} \times I_{CC} \tag{4}$$

The dynamic power consumption of a CMOS device is calculated by adding the transient power consumption and capacitive-load power consumption.

Transient Power Consumption

The transient power is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This power is a result of the current required to charge the internal nodes (*switching current*) plus the current that flows from V_{CC} to GND when the p-channel and n-channel transistors turn on briefly at the same time during the logic

transition (through current). The frequency at which the device is switching, plus the rise and fall time of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible in comparison with the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the device and the charge and discharge current of the load capacitance. The transient power consumption can be calculated using equation 5.

$$P_{\rm T} = C_{\rm pd} \times V_{\rm CC}^2 \times f_{\rm I} \times N_{\rm SW} \tag{5}$$

In case of single-bit switching, Nsw in equation 5 becomes 1.

Capacitive-Load Power Consumption

Additional power is consumed in charging of external load capacitance and is dependent on switching frequency. Equation 6 can be used to calculate this power while all outputs have the same load and are switching at the same output frequency.

$$P_{L} = C_{L} \times V_{CC}^{2} \times f_{O} \times N_{SW} (C_{L} \text{ is the load per output})$$
(6)

In case of different loads and different output frequencies at all outputs, equation 7 is used to calculate capacitive-load power consumption.

$$P_{L} = \Sigma (C_{Ln} \times f_{On}) \times V_{CC}^{2}$$

$$(7)$$

Therefore, dynamic power consumption (P_D) is the sum of these two power consumptions, and is expressed in equation 8 (single-bit-switching case) and 9 (multiple-bit switching with variable load and variable output frequencies):

$$P_{D} = \left(C_{pd} \times f_{I} \times V_{CC}^{2}\right) + \left(C_{L} \times f_{O} \times V_{CC}^{2}\right) \tag{8}$$

$$P_{\rm D} = \left[\left(C_{\rm pd} \times f_{\rm I} \times N_{\rm SW} \right) + \Sigma \left(C_{\rm Ln} \times f_{\rm O_{\rm n}} \right) \right] V_{\rm CC}^{2}$$
(9)

Total power consumption with a CMOS-level input is the sum of static and dynamic power consumption.

TTL-Level Inputs

Similarly, with TTL-level inputs, both static and dynamic power consumption can be calculated using equations 10, 11, and 12.

$$P_{S} = V_{CC}[I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_{d})]$$
(10)

$$P_{D} = (C_{pd} \times f_{I} \times V_{CC}^{2}) + (C_{L} \times f_{O} \times V_{CC}^{2}) \text{ (single-bit switching)}$$
(11)

$$P_{D} = \left[\left(C_{pd} \times f_{T} \times N_{SW} \right) + \Sigma (C_{Ln} \times f_{On}) \right] V_{CC}^{2}$$
(multiple-bit switching with variable load and frequency)

BICMOS

Static Power

$$P_{S} = V_{CC} \left\{ DC_{en} \left[\left(N_{H} \times \frac{I_{CCH}}{N_{T}} \right) + \left(N_{L} \times \frac{I_{CCL}}{N_{T}} \right) \right] + (1 - DC_{en})I_{CCZ} + (N_{TTL} \times \Delta I_{CC} \times DC_{d}) \right\}$$
(13)

Where:

 $\Delta I_{CC} = 0$ for bipolar devices

NOTE:

For a continuous waveform at 50% duty cycle, $DC_{en} = 1$.

Equation 13 becomes:

$$P_{S} = V_{CC} \left[\left(N_{H} \times \frac{I_{CCH}}{N_{T}} \right) + \left(N_{L} \times \frac{I_{CCL}}{N_{T}} \right) \right]$$
(14)

NOTE:

If half of the time the waveform is high and half of the time the waveform is low and the waveform is switching continuously, \Rightarrow (N_H = N_L = 1/2 N_T), P_S becomes:

$$P_{\rm S} = \left(\frac{V_{\rm CC}}{2}\right) (I_{\rm CCH} + I_{\rm CCL}) \tag{15}$$

Dynamic Power

$$P_{D} = (DC_{em} \times N_{SW} \times V_{CC} \times f \times I_{CCD}) \text{ Condition is 50 pF-} \parallel 500 \Omega$$

 I_{CCD} is calculated with 50 pF \parallel 500 Ω , and given number of outputs switching.

NOTE:

For a continuous waveform at 50% duty cycle, $DC_{en} = 1$.

Dynamic power with external capacitance:

$$P_{D} = DC_{en} \times N_{SW} \times V_{CC} \times f \times (V_{OH} - V_{OL}) \times (C_{L} - 50 \text{ pF}) + DC_{en} \times N_{SW} \times V_{CC} \times f \times I_{CCD}$$
(17)

 I_{CCD} is calculated with 50 pF \parallel 500 Ω , and given number of output switching.

Power is also consumed by the upper output driver due to the output resistor (500 Ω in most load circuits for outputs in the data sheet). This power is very small but must be included in the dynamic power consumption calculation. Equation 18 is used to calculate this power consumption.

$$P_{\text{Res}} = (V_{\text{CC}} - V_{\text{OH}}) \times \frac{V_{\text{OH}}}{R}$$
(18)

NOTE:

Assume that the output waveform is always at logic high and is not frequency dependent.

Therefore, total dynamic power consumption is:

$$P_{D_TOT} = P_D + P_{_Res}$$
 (19)
Finally, total power consumption can be calculated as:

$$P_{\text{_Total}} = P_{\text{D_TOT}} + P_{\text{S}}$$
 (20)

any one of these is beneficial. A reduction in lower consumpting provides several other benefits, Less bent is generated . send W reduces problems associated with high temperature, such as the need for hearsinks. This provides the consumer with a modulor

V_{CC} = supply voltage (V)

ICC = power-supply current (A) (from the data sheet)

= power-supply current when outputs are in low state (A) (from the data sheet)

= power-supply current when outputs are in high state (A) (from the data sheet)

= power-supply current when outputs are in high-impedance state (A) (from the data sheet)

= power-supply current when one input is at a TTL level (A) (from the data sheet)

DC_{en} = % duty cycle enabled (50% = 0.5)

 DC_d = % duty cycle of the data (50% = 0.5)

= number of outputs in high state

= number of outputs in low state = total number of outputs switching

= total number of outputs

= number of inputs driven at TTL levels

 f_{T} = input frequency (Hz)

= output frequency (Hz) f_{O}

= operating frequency (Hz)

V_{OH} = output voltage in high state (V)
V_{OI} = output voltage in low state (V)

C_I = external-load capacitance (F) as most of (TM SU = M = MM) as Alauounituos anidativa ai

 I_{CCD} = slope of the I_{CC} versus frequency curve (A/Hz × bit)

C_{I (eff)} = effective-load capacitance (F)

 $f_{\rm I}$ = ratio of output and input frequency (Hz)

P_T = transient power consumption
P_D = dynamic power consumption
P_S = static power consumption

P_Res = power consumption due to output resistance | b settmen nevro Long Ω 000. 13q 00 draw beneficially at quart

PD TOT = total dynamic power consumption

P Total = total power consumption

C_{PD} = dynamic power dissipation capacitance (F)

P_I = capacitive-load power consumption

 Σ = sum of n different frequencies and loads at n different outputs

f_{On} = all different output frequencies at each output numbered 1 through n (Hz)

C_{I,n} = all different load capacitances at each output numbered 1 through n

For GTL and BTL/FB devices, the power consumption/calculation is similar to a BiCMOS device with the addition of the output power consumption through the pullup resistor, since GTL is open drain and BTL/FB is open collector.

The total power calculated using these equations should be less than the package power dissipation mentioned in the data sheets. Otherwise, the device might not function properly.

Benefits of Minimizing Power Consumption

Power consumption can be minimized in a number of ways. DC power consumption can be reduced to leakage by using only CMOS logic, as opposed to bipolar and BiCMOS logic. The leakage, in turn, is proportional to the area of diffusion, so the use of minimum-size devices is an advantage. Dynamic power consumption can be limited by reducing supply voltage, switched capacitance, and the frequency at which the logic is clocked. Supply voltage tends to be a system design consideration, and low-power systems use 1.5-V to 3.3-V supplies.

Power consumption is a function of the load capacitance, the frequency of operation, and the supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several other benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heatsinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device, and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

Reliability Implications

The integrated-circuit component power dissipation during operation elevates the device junction temperature. The thermal impedance (θ_{JA} or k-factor) of a device package is defined as the increase in the junction temperature, above ambient temperature, due to the device power dissipation. Thermal impedance is measured in degrees Celsius per watt. Thermal characteristics of a device package are commonly described using two indices, Q_{JA} (junction to ambient) and Q_{JC} (junction to case). Controlling the junction temperature within a desired range is critical for proper device functionality and long-term reliability.

Table 4, based on long-term sustained temperatures, shows the relationship between junction temperature and predicted failure rate.

Table 4. Junction Temperature Versus 100,000-Hour Predicted Failure Rate

JUNCTION TEMPERATURE (°C)	FAILURE RATE (%)
100	0.02
110	1
120	11
130	46
140	80
150	96

Higher component temperatures increase the possibility of component wearout due to such failure mechanisms as electromigration and ball-bond intermetallic failures.

Thermal Definitions

Heat	A form of energy associated with the motion of atoms or molecules in solids, and capable of being
	transmitted through solid and fluid media by conduction, through fluid media by convection, and

through empty space by radiation

Conduction Heating The most commonly recognized form of heat transfer. Metal materials are good conductors of heat and

can be quantified by a proportionality constant (k), also known as thermal conductivity. The higher the thermal-conductivity number, the more quickly heat transfer, by means of conduction, occurs. Leadframes are the primary media for conduction heating in plastic-encapsulated devices; however,

mold compound materials play a major role in this type of heat transference.

heating. This type of heat transfer is most commonly seen when air is forced across a heated surface, resulting in the cooling of the heat source. Heat is transferred to the air by means of convection heating. The rate of heat transfer depends on the surface area of the heat source and the velocity and physical properties of the airflow. When a device package is generating heat through normal operation, the

device can be cooled by applying a constant airflow across the surface of the package.

Radiant heat transfer occurs between two objects separated within a vacuum.

Ambient Temperature The temperature of the surrounding air, usually used as a reference point to calculate the junction or

case temperature. This temperature is measured at some specific distance from the device.

Case Temperature The temperature on the package surface measured at the center of the top of the package

Junction Temperature The temperature of the die inside the device package

Acknowledgment

The authors of this report are David Holmgreen, Doug Romm, Abul Sarwar, and Ron Eller. The thermal-model program, ThermCAL, was developed by Darvin Edwards.

References

- 1 Electronic Industries Association, EIA/JEDEC Std JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages, August 1996.
- 2 Darvin Edwards, "Thermal Analysis Using FEA (v1.1)," November 1991.
- 3 Darvin Edwards, "Development of JEDEC Standard Thermal Measurement Test Boards."

lectronigration and hall-bond intermetable failures.

A form of energy associated with the motion of mons or molecules in solids, and capable of being transmitted through solid and fluid meths by conduction, through fluid media by convection, and through empty space by radiation.

The most commonly recognized form of host transfer. Metal materials are good conductors of host and through empty space by radiation.

Sanduction Feating.

The most commonly recognized form of host transfer. Metal materials are good conductors of host and thermal-conductivity number, the more quickly bear transfer, by means of conduction, occurs them and compound materials play a major rele in this type of heat transfer the most commonly seen when aft is forced across a heated surface.

The heat transfer be that transfer is most commonly seen when aft is covered across a heated surface from the cooling of its hast source. Heat is transferred to the airby means of convection heating properties of the fairflow. When a device prockets is generating heat through normal operation devices on the cooled by applying a constant airflow across the surface of the package.

The representative of the surrounding air, usually used as a reference point to calculate the junction of the programme. The representative of the surrounding air, usually used as a reference point to calculate the junction of the surrounding air, usually used as a reference from the device.

The temperature. This temperature is measured at some opening distance from the device.

The temperature of the surrounding surface measured at some opening of the package.

The temperature of the surrounding surface measured at the center of the top of the package.

The temperature of the surrounding the device accidence.

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Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading, regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.

EXAMPLE: SN 74LVTH162244 DGG Prefix SN = Standard prefix SNJ = Compliant to MIL-PRF-38535 (QML) **Unique Circuit Description** MUST CONTAIN EIGHT TO FIFTEEN CHARACTERS Examples: 74LVTH125 74LVTH16952 74LVTH162541 Package MUST CONTAIN ONE TO THREE LETTERS = plastic small-outline package DB, DL = plastic shrink small-outline package DCK = plastic small-outline transistor package DGG, PW = plastic thin shrink small-outline package DGV = plastic thin very small-outline package FK = ceramic chip carrier J, JT = ceramic dual-in-line package W, WD = ceramic flat package (from pin-connection diagram on individual data sheet) Tape and Reel Packaging Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

valid for surface-mount packages only. All orders for tape and reel must be for whole reels

Blank = Not taped and reeled R = Reeled product[†]

† All reeled material previously designated LE continues to be reeled left embossed, but an R designator is used.



Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading, regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.

Prefix

SN = Standard prefix

SNJ = Compiliant to Mil.-PRF-S8635 (OML)

MUST CONTAIN EIGHT TO FIFTEEN CHARACTERS

Examples: 74LVTH1855

TALVTH185541

Package

D, DW = plastic small-outline package

DB, DL = plastic shrink small-outline package

DGC, PW = plastic shrink small-outline package

DGC, PW = plastic thin straks small-outline package

DGC, PW = plastic thin straks small-outline package

DGC, PW = plastic thin straks small-outline package

DGV = plastic thin straks small-outline package

DGV = plastic thin straks small-outline package

U, JT = ceramic duel-in-line package

J, JT = ceramic duel-in-line package

V, WD = ceramic duel-in-line package

(from pin-connection diagram on Individual data sheet)

Valid for surface-mount packages only. All orders for tage and neel must be for whole mels.

Rlants = Not traved and recised

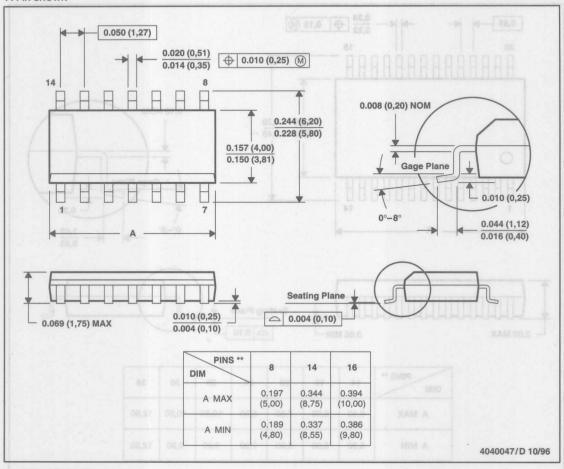
TAII meted material previously designated LE continues to be recied left embossed, but an Pi designator is utad.



D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

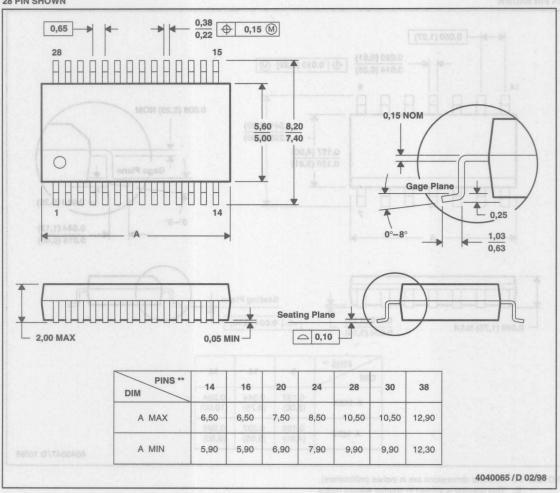
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

28 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

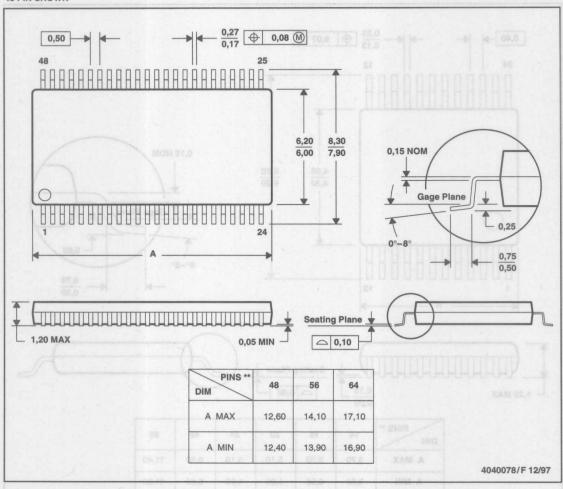
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

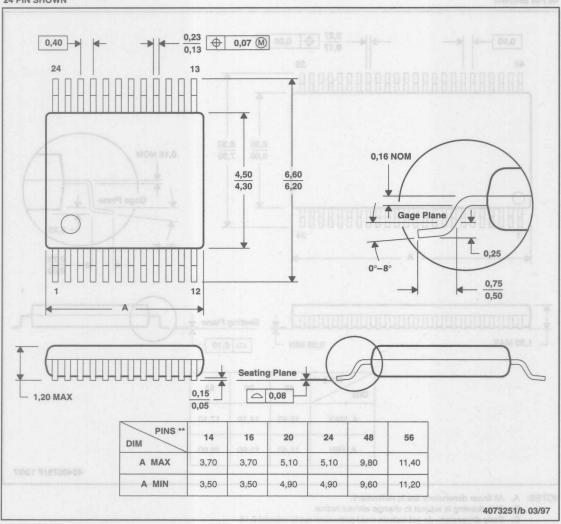
C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

24 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

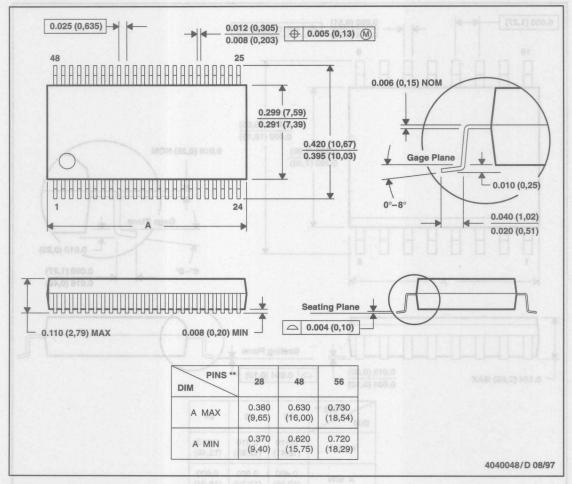
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. The 24 and 48 pins falls within JEDEC MO-153 and the 14, 16, 20, and 56 pins falls within JEDEC MO-194.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48-PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

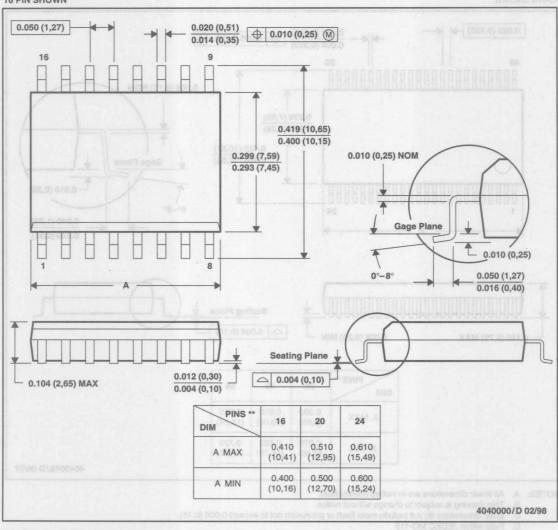
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

DW (R-PDSO-G**)

16 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters). B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

FK (S-CQCC-N**)

28 TERMINAL SHOWN

B SQ 22

A SQ

19

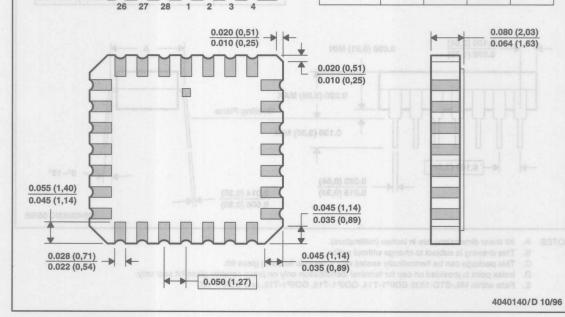
20

23 24

25

LEADLESS CERAMIC CHIP CARRIER

NO. OF		Α	В			
TERMINALS	MIN	MAX	MIN	MAX 0.358 (9,09) 0.458 (11,63) 0.560 (14,22) 0.560 (14,22)		
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)			
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)			
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)			
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)			
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)		
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)		



11

(10

9

8

6

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

18 17 16 15 14 13 12

D. The terminals are gold plated.

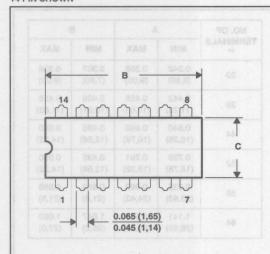
E. Falls within JEDEC MS-004



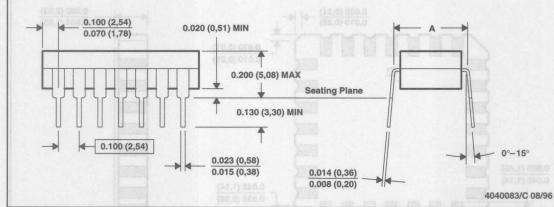
J (R-GDIP-T**) O OMAREO SEEJGAEJ

14 PIN SHOWN

CERAMIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20	
A MAX	0.310	0.310	0.310	0.310	
	(7,87)	(7,87)	(7,87)	(7,87)	
A MIN	0.290	0.290	0.290	0.290	
	(7,37)	(7,37)	(7,37)	(7,37)	
в мах	0.785	0.785	0.910	0.975	
	(19,94)	(19,94)	(23,10)	(24,77)	
B MIN	0.755 (19,18)	0.755 (19,18)		0.930 (23,62)	
C MAX	0.280	0.300	0.300	0.300	
	(7,11)	(7,62)	(7,62)	(7,62)	
C MIN	0.245	0.245	0.245	0.245	
	(6,22)	(6,22)	(6,22)	(6,22)	



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a ceramic lid using glass frit.

D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, and GDIP1-T20

JT (R-GDIP-T**)

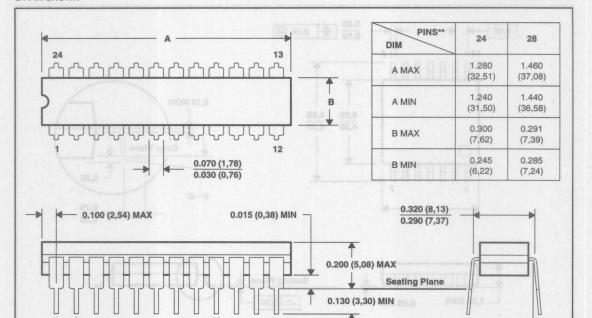
24 PIN SHOWN

CERAMIC DUAL-IN-LINE PACKAGE

0°-15°

4040110/C 08/96

0.014 (0,36)



NOTES: A. All linear dimensions are in inches (millimeters).

0.100 (2,54)

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a ceramic lid using glass frit.

D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

0.023 (0,58)

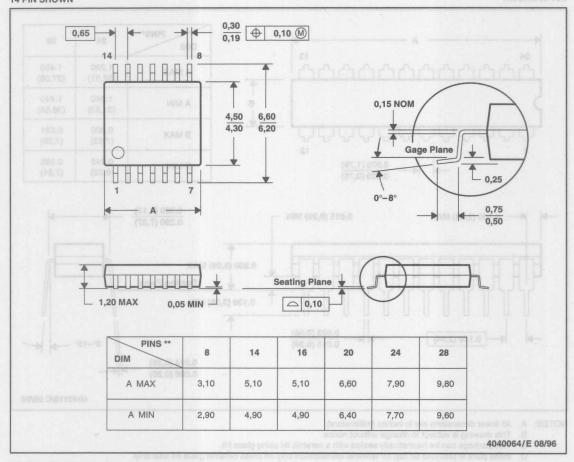
0.015 (0,38)

E. Falls within MIL STD 1835 GDIP-T24, GDIP-T28 and JEDEC MO-058 AA, MO-058 AB.

PW (R-PDSO-G**)

14 PIN SHOWN

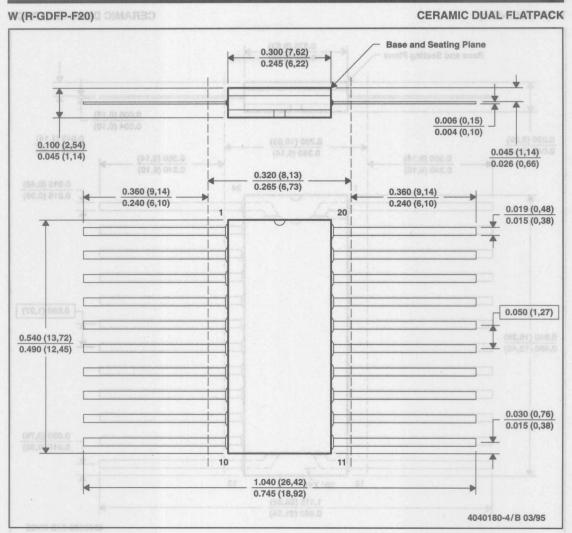
PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153



NOTES: A. All linear dimensions are in inches (millimeters).

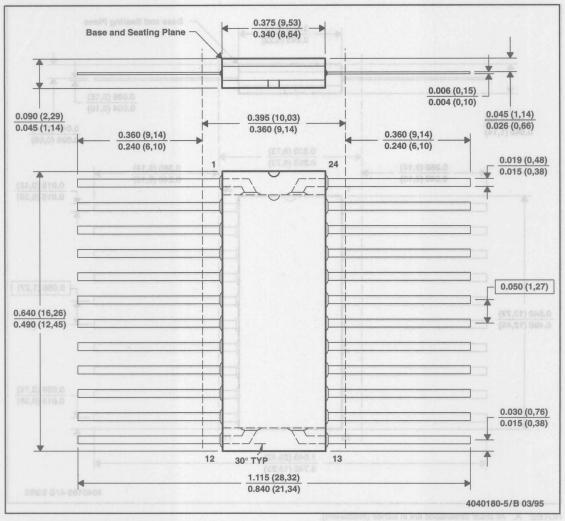
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD-1835 GDFP2-F20



W (R-GDFP-F24)

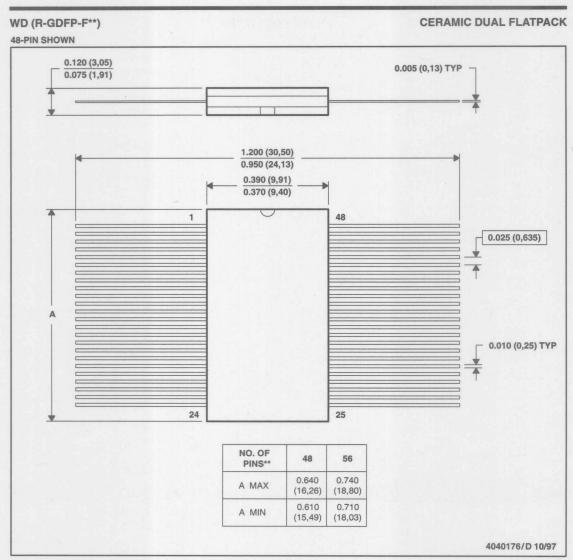
CERAMIC DUAL FLATPACK



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
- E. Index point is provided on cap for terminal identification only.





NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a ceramic lid using glass frit.

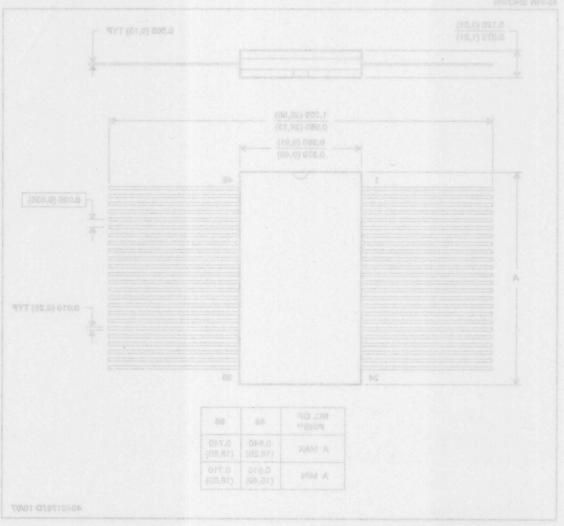
D. Index point is provided on cap for pin identification only

E. Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA

GDFP1-F56 and JEDEC MO-146AB







- C. This package can be hermatically sealed with a cotamic lid using gless int.

 D. Index point is provided on cap for pin identification only

 E. Falls within MIL-STD-1638: GDFP7-F48 and JEDEC MO-146AA

